Improved ranking list classifier for analog circuts fault diagnosis

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Abstract **Simple fault diagnosis strategy based on the GRA-type (Grey Relational Analysis) algorithm with improved final classification procedure and using modified feature selection method is presented and discussed. Procedure enabling us to detect and localize single and multiple catastrophic faults, is prepared under assumption that input data sets are extracted from DC analysis of circuits having limited access to the internal nodes.**

Keywords **analog circuits, fault diagnosis, classifiers, elements' tolerance, data mining, feature selection.**

I. Introduction

Fault diagnosis and testing of analog circuits with elements' tolerances included has grown into a special field of interest in semiconductor industry, and seem to be still an important part of modern modeling, designing and manufacturing process. In opposite to digital part of "mixed signal circuits", methodologies for testing analog integrated circuit are relatively unexplored. Considering, that testing represents a key cost factor (up to 70%) of the production process, optimal diagnostic strategies, fast and accurate enough, are in big request and can give substantial competitive edge in the market.

The parameters variations may be taken into account by using tolerance regions calculations [1] or particular classifiers including tolerance in the learning stage of pattern recognition process. Most recently, the algorithms based on grey relational data analysis [2] were introduced to the analog circuit fault diagnosis [3], [4]. Unfortunately, these very fast and simple techniques, do not ensure good efficiency for circuits with large variations of elements' parameters.

Simple fault diagnostis strategy based on the GRA-type algorithm with improved final classification procedure and using modified feature preselection method is presented and discussed. Algorithm enabling to detect and localize single and multiple catastrophic faults, is prepared under assumption that input data sets are extracted from DC analysis of circuits having limited access to the internal nodes.

II. Results

The main classifying procedure proposed in the paper is based on the concept presented in details in [3] and [4]. There, successful implementation of some grey systems theory elements [2] was proposed for analog circuit fault diagnosis.

Let us consider the set of data followed from circuit under test measurement simulations:

$$\boldsymbol{x}_j^{k(i)} \in X, k = 1,2,...,N, \quad j = 1,2,...,M, \, i = 1,2,...,T \tag{1}$$

where N is a number of features (test points) defined for the investigated circuit, M – number of all circuit's states, including nominal one, T denotes the number of Monte Carlo trials. Hence, x_j^k defines k-th feature of the investigated j-th circuit state belonging to the i-th simulation. Then, T different sets of rational degrees [3] are defined for the assumed elements' tolerance:

$$\Gamma_j^{(i)} = \frac{1}{N}\sum_{k=1}^{N} \gamma_{jk}^{(i)} \tag{2}$$

Winning states of all T trials are gathered and one of them is chosen as CUT's (circuit under test) fault by use of elaborated special procedure. To improve the behaviour of the classifier, authors proposed also features selection algorithm based on GA optimisation of the fitness function containing between-class average distance, within-class dispersion [5] and GRA classifier quality factor [4].

Simulations of the Darlington benchmark circuit (15 defined faults and 21 initial features) shown in Fig.1 confirm, that efficiency of the proposed improved procedure for tolerances 2%-10% increases about 8-10% in comparison with the previous implementations of the method and achieved satisfactory level of 96-97%.

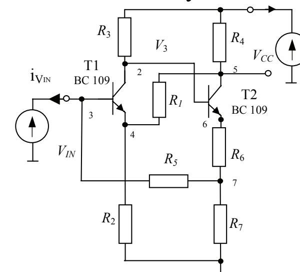

Fig. 1. The Darlington benchmark circuit [3],[4],[5]

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