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Dual 11-Bit Current-Steering D/A Converter for the Transmission of I-Q Encoded Information

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Abstract:
This paper presents the design of an 11-bit dual D/A converter for the transmission of I-Q encoded information. The intended field of application is the automotive industry. Therefore the specific environmental hazards had to be considered, primarily the wide operating temperature range. The design is in the ON Semiconductor smart power 350 nm CMOS technology. The main function of the converter is to transmit information encoded into I-Q signal representation. The I and Q signal paths are in reality represented with sine and cosine signals. In addition, this information can have the maximum change rate of 3000 rps. The decomposition of transmitted information is expected to occur at the receiver side in the I-Q decoder block. To comply with these requirements the D/A converter has to be dual (sine and cosine), bipolar and of a segmented current-steering architecture (best accuracy/area tradeoff). Goals have been respectively selected to have DNL < ± 0.5 LSB (to guarantee monotonicity) and INL < ± 3 LSB in order to achieve acceptable linearity. Channel gain mismatch has to be better than 1 % to fulfill the dual channel accuracy requirement, calculated from the sensitivity of the output error on the signal amplitude mismatch. Special attention has been paid to the layout placement of the current steering matrix elements and to the switching strategy as well. The article provides design overview with the measurement results of the manufactured prototype.

INTRODUCTION

D/A converters have become essential building blocks of mixed signal integrated circuits. Numerous articles and papers have been published regarding the D/A converter principle and a large amount of topologies has been introduced [1]-[2]. The proper architecture selection has to be made with respect to the D/A requirements such as conversion speed, accuracy and, most importantly, the tradeoff between performance area. A good compromise can be achieved with the proper selection of the architecture segmentation level [3]. The main function of the proposed DAC is depicted in Fig. 1

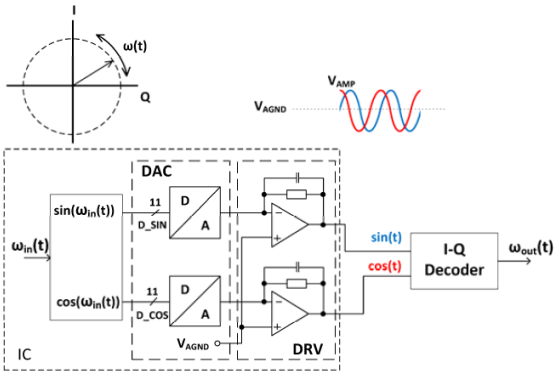

Fig. 1: Functional overview of the converter

The input information represented with digital control word is passed to D/A and is consequently converted into the analog current representation. An output D/A current is then converted into the output voltage in the output driver block. In addition, this block accommodates the role of a reconstruction filter.

As previously mentioned the angular vector can be evolving in time.

1. D/A CONVERTER CORE

The top level block diagram of the proposed D/A converter is shown in Fig. 2. The topology includes two identical current source matrices, one per channel, two current mirroring circuits and common reference current generator with reference voltage block. The D/A conversion is done in the current matrix and current, equivalent to the input D/A conversion word, is switched either directly to the driver input or to the current mirroring block input according to the input sign of the conversion word. Generation of the opposite sign current is performed within the high precision current mirroring block. This block accommodates a simple current mirror with additional dedicated dynamically switched circuitry. Further details of the operation will be discussed in section 1.2. This circuitry has been chosen with respect to the maximum change rate of the processed information and with consideration of the maximum allowed gain error.

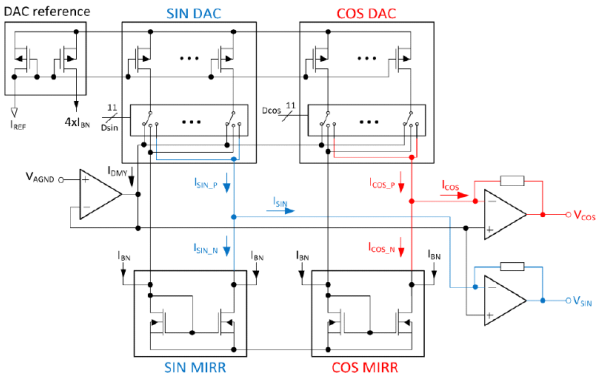

Fig. 2: Converter core block diagram

Reference current generator block provides HIPO (High-Ohmic Poly-Silicon) current bias created from a precise band-gap voltage reference applied over the HIPO resistor and the same type of the resistor is used as a driver feedback resistor. Therefore the output signal amplitude is insensitive to the process variation.

1.1. CURRENT SOURCE MATRIX

The current source matrix block shown in is essentially of a segmented current-steering architecture. A specialty of this particular architecture is the fact that the current mirroring is done with a unitizing strategy also in the binary weighted branches (BCD) part. This has been done in order to relax the required minimum current mismatch [4] of a unit transistor as it would be in case when the binary weighting had been done in the ordinary way, via the proper binary-weighted W/L sizing of the BCD part transistors. In practice this would lead to a very low steered current in the LSB branch, and consequently much larger area would have been occupied compared to this presented architecture. The segmentation of current source elements is depicted in . The unary part contains 63 unary and 4 BCD current branches. Sizing of the transistors has been chosen with respect of the maximum allowed random matching error derived from the well-known Pelgrom formula [4] valid for MOS transistors operating in strong inversion

$$\sigma\left(\frac{\Delta I}{I}\right)^2 = \sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + \frac{4\cdot\sigma(\Delta V_t)^2}{(V_{GS}-V_t)^2},$$

where

$$\sigma\left(\frac{\Delta\beta}{\beta}\right)^2 = \frac{A\beta^2}{W\cdot L};\quad \sigma(\Delta V_t)^2 = \frac{AVt^2}{W\cdot L}.$$

The W/L ratio of the unary part transistors are 2-times bigger since they need to have the same Gate Source voltage while delivering twice the current compared to the binary branch ones. Since the current through all BCD branches has the same value the binary weighting is performed at the R-2R resistive network current divider. The resistance between the neighboring current mirror branches has a resistance of R and the resistance to the reference voltage net has a resistance of 2×R, where R is the resistance of the unit element resistor. With this topology the current division by 2 occurs from the right side LSB branch (b0) towards the leftmost BCD branch current output. The main advantage is the fact that with this configuration geometric dimensions of all transistors in BCD branches are of the same size, and more importantly, the mismatch contribution of all elements is the same as well. Moreover, the mismatch

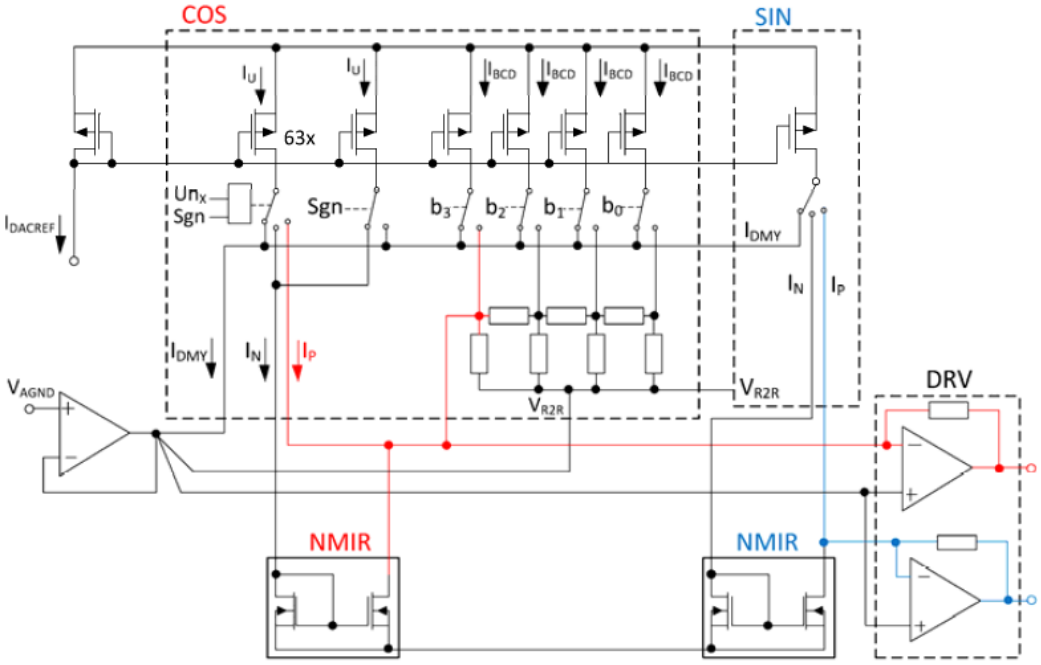

Fig. 3: Converter current-steering architecture

contribution to the output current is reduced since the relative sensitivity is reduced by the corresponding binary weight so the relaxing of the mismatch requirement is possible. Another advantage is that, with the same sizing, the resulting placement of the unit elements can be much more effective. The physical layout of the particular current mirror elements is done by placing all current elements from both channels side by side in one single matrix and by choosing their positions respecting the linear gradient error effects [5]. This placement is expected to minimize the overall effect of systematic mismatch error contributors, e.g. package surface stress and temperature gradient, but the main motivation was to reduce the sine vs cosine channel amplitude mismatch.

1.2. PRECISE CURRENT MIRROR

The dual polarity of the current D/A converter is accomplished with a special precise current mirroring circuitry. Such a mirroring concept has been chosen with respect to the negative impact of the parasitic Gate-Source capacitance on the evolving signal. This is primarily due to the minimum required area of one unit mirroring transistor considering required current mirror precision < 1 %. This parasitic capacitance would cause that, from a certain speed, part of the converter current would be reduced by this parasitic capacitive charge current, resulting in additional speed dependent amplitude error. Modified Dynamic Element Matching (DEM) technique has been introduced to overcome this phenomenon. The principle of the DEM current mirror is discussed in [1] and the final implementation and operation principle is shown in Fig. 4 and Fig. 5 .

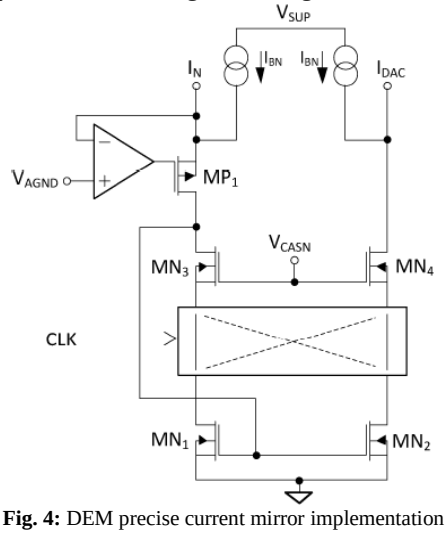

Fig. 4: DEM precise current mirror implementation

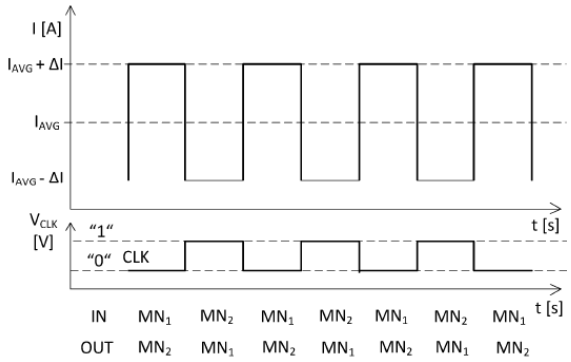

Fig. 5: DEM operation principle

The current mirror outputs of the transistor elements are being periodically interchanged between the input and output. This DEM operation has allowed the size of the mirroring transistors to be much smaller. The dimensions of the mirroring transistors have been selected to minimize the parasitic Gate Source capacitance while some finite acceptable current mirroring error is created. However, with the application of the DEM technique the finite static error will be significantly decreased by the dynamic operation depicted in Fig. 5. In spite of the dynamic operation a small amount of residual error will be still present at the current mirror output. This residual ripple can be very effectively eliminated in the reconstruction filter and the suppression is given by the attenuation of the filter at properly selected DEM switching frequency. Since the circuit has to handle high dynamic range input current, special care has been be taken to the correct DC operating point of the mirroring transistors. The high dynamic current range also led to the need of an additional dc current injection into both branches with an amount of 10 % of the maximum processed current. A unity gain voltage buffer with P-MOS transistor, acting as a voltage cascode, had been added at the input to maintain the same voltage conditions at both D/A converter current outputs.

2. PROTOTYPE MEASUREMENT

The manufactured prototype has been validated with manual AC and DC measurements at temperature 27°C. Dynamic measurement has been performed with input harmonic signal with frequency of 3 kHz. Resolution of the waveform generator has been 14 bits. Measurement has been repeated 20 times in order to suppress the background noise contribution. Resulting signal spectra is depicted in Fig. 6 with outcome SFDR=69 dBc, SINAD=58 dBc, THD=66 dB, ENOB=9.34 Bit. Suppression of the image signal frequency ~92 dBc.

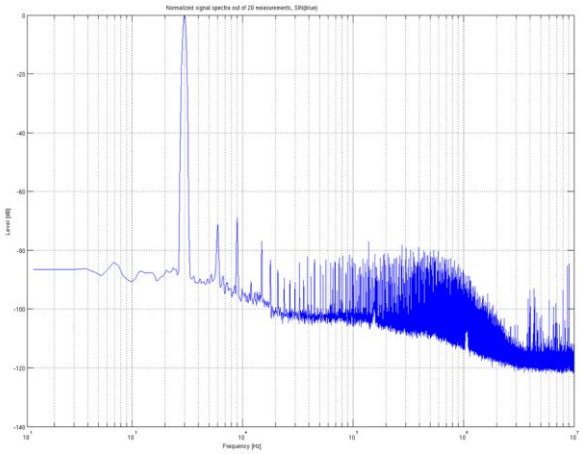

Fig. 6 Converter output frequency spectra of 3 KHz input signal

Purpose of the DC measurement has been to validate the static linearity performance (INL, DNL) of the converter with and without DEM and also to validate the effect of the current matrix layout placement. Measured INL characteristics are shown in Fig. 7.

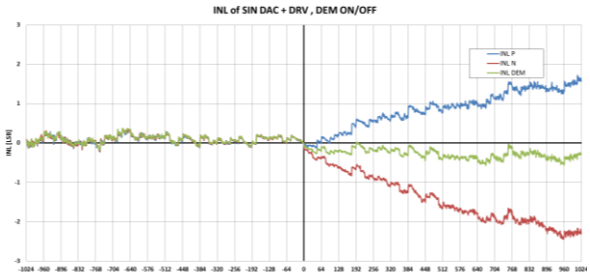

Fig. 7 Converter INL characteristic comparison with (middle green) and without DEM (top blue, bottom red)

It is clear that the DEM has significantly improved the linearity of the converter from INL ~2.8 LSB down to INL~ 0.5. As a conclusion DEM concept has been validated with positive result. Testing has also been executed on the ATE (Automatic Tester Equipment) so statistical measurement data are available for selected important parameters, e.g. channel gain mismatch, polarity gain error SFDR, THD, ENOB. The summary of selected ATE measurement results is in Table 1. The results confirm the expected D/A converter performance.

Parameter	***@27 °C***	***@180 °C***	***Unit***
DNL	±0.3	±0,28	LSB
INL	0.5	0.4	LSB
Gain error	0.041	0.042	%
SFDR	69	68	dBc
THD	66	65	dB
ENOB	9.36	9.31	Bit

Table 1 Summary of D/A measruement results

CONCLUSION

The designed 11-bit DAC with DEM current mirroring circuitry and with modified switching sequence has been designed in the smart power CMOS ON Semiconductor technology. This converter is capable of operation under extreme temperature conditions from -40 to 180℃, which is characteristic for the automotive environment. The validation of proposed D/A converter has been done with satisfying results.

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