Chips for discovering the Higgs boson and other particles at CERN: present and future

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Abstract – **Integrated circuits and devices revolutionized particle physics experiments, and have been essential in the recent discovery of the Higgs boson by the ATLAS and CMS experiments at the Large Hadron Collider at CERN [1,2]. Particles are accelerated and brought into collision at specific interaction points where detectors, giant cameras of about 40 m long by 20 m in diameter, take pictures of the collision products as they fly away from the collision point. These detectors contain millions of channels, often implemented as reverse biased silicon pin diode arrays covering areas of up to 200 m^2 in the center of the experiment, generating a small (~1fC) electric charge upon particle traversals. Integrated circuits provide the readout, and accept collision rates of about 40 MHz with on-line selection of potentially interesting events before data storage. Important limitations are power consumption, radiation tolerance, data rates, and system issues like robustness, redundancy, channel-to-channel uniformity, timing distribution and safety. The already predominant role of silicon devices and integrated circuits in these detectors is only expected to increase in the future.**

Keywords-particle detection; silicon pin diodes; charge sensitive readout

I. INTRODUCTION

Physics research on the nature of matter has culminated in the standard model, postulating that all matter in the universe is constructed from a few elementary particles interacting by four fundamental forces. This model explains almost all experimental results observed in nature. Many experimental observations that contributed to the standard model, have been obtained in experiments where particles are first accelerated and then brought into collision at specific interaction points. This was also the case for the recent discovery at CERN by the ATLAS [3] and CMS [4] experiments of the Higgs boson explaining the origin of mass of the elementary particles. The thousands of fragments produced by these collisions are detected and visualized by detectors about 40 m long and 20 m in diameter constructed around these interaction points. The Large Hadron Collider or LHC at CERN accelerates protons or heavier ions in a ring in a tunnel at about 100 m underground of about 27 km circumference. Fig 1 shows an aerial photo indicating the position of the ring and the main experiments. References [1] and [2] describe the role of integrated circuits and detectors in these experiments in detail. In the following this is summarized, followed by an overview of the main challenges in the future.

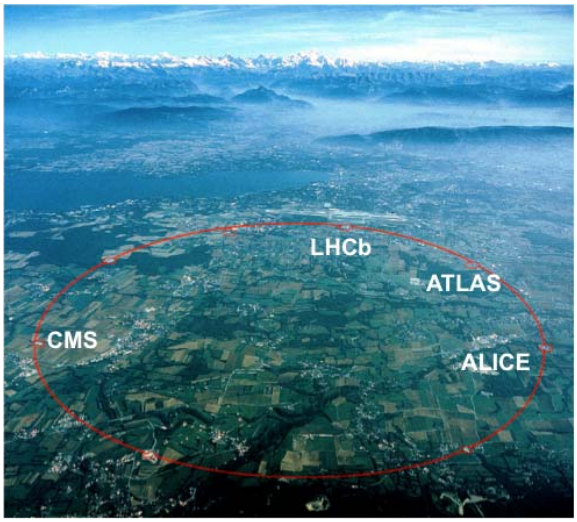

Figure 1. Aerial view of CERN indicating the location of the 27 km LHC ring with the position of the main experimental areas the ring. The city of Geneva, its airport, the lake and Mont Blanc are visible © 2015 CERN.

II. MAIN CONSTRAINTS AND LIMITATIONS

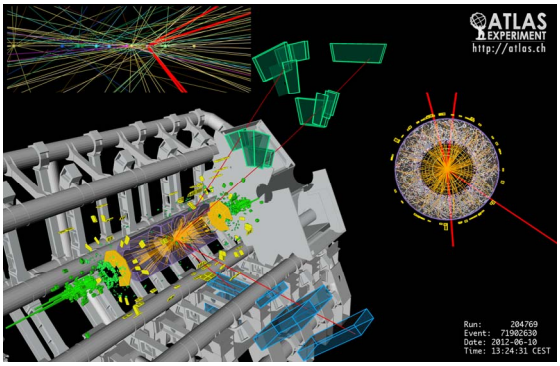

Figure 2. A candidate event for a Higgs decay into four muons, recorded in ATLAS on June 10th, 2012. ATLAS Experiment © 2012 CERN.

Physics interest often lies in rare events: for instance a candidate for a Higgs event was produced in the last run at LHC in less than one out of 10^{12} collisions, requiring to produce proton collisions at a sufficiently high rate, 40 MHz at the LHC. This has several implications:

- the radiation load is dominated by non-interesting events, orders of magnitude higher than what is required for space: 1 MGy or 100 Mrad ionizing radiation and 10^{15} 1 MeV neutron equivalent/cm^2 of

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non-ionizing particle flux for the inner detector layers at a few cm radius and roughly inversely proportional to the square of the distance (radius) to the interaction point. Services need to be housed in a counting room separated from the detector by a thick wall to allow access during running. Certain parts of the detector can only be accessed during long shutdowns, and need remote monitoring and control and an automatic safety system to intervene if some parameters are observed to exceed safe limits.

- A 25 ns time resolution is needed to associate particle traversals with the correct bunch crossing. New collisions take place before all fragments generated by the previous bunch crossing have left the detector, requiring correction for particle travel time.

- One cannot read nor store all events: 1 MB per event at 40 MHz corresponds to a raw data rate of 40 TB/s. On-line event selection is carried out in a few microseconds in Field Programmable Gate Arrays (FPGAs) in the counting room to generate a signal to trigger full detector readout. In ATLAS and CMS the maximum level 1 trigger rate is 100 kHz. Further event selection is carried out in computer banks before writing ~1GB/s to disk.

Figure 2 shows a candidate event for a Higgs boson decay in four muons recorded in ATLAS in 2012. The inset on the right-hand side shows a zoom of the tracking detector. The inset on top shows a zoom of the center area, indicating the four muons originate from the same point in space. The figure illustrates the event complexity and the challenge to select the very few interesting ones out of many produced.

III. PRESENT PHYSICS EXPERIMENTS

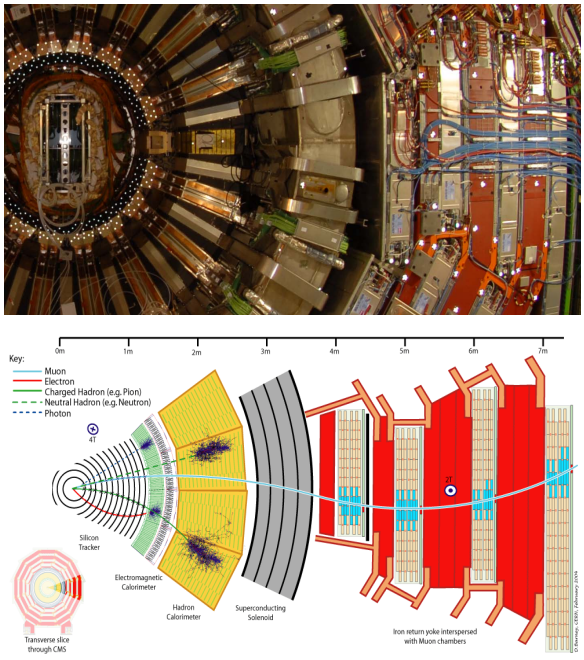

Figure 3. Front view of the CMS detector (top) with schematic overview of the different layers (bottom). The scale in meters indicates the distance (radius) from the interaction point. Only the muon detectors are outside of the solenoid generating the 4 T magnetic field. CMS Experiment © 2015 CERN.

Detectors consist of multiple layers to visualize and identify the fragments coming of the collisions. Figure 3 shows a front view of the CMS detector: the beams come in in the center of the detector (on the left in the picture), perpendicular to the page. The inner layers are used to reconstruct the track of charged particles curved due to the presence of a magnetic field (4 T in CMS) parallel to the two incoming beams. More outer layers measure the energy of the particles. The outermost layers detect muons, highly penetrating particles which are often the signature of interesting events.

The ATLAS detector is 44 m long, measures 22 m in diameter and weighs 7000 tons. CMS measures 22 m in length and 15 m in diameter and weighs 12 500 tons. Such dimensions are required to provide sufficient resolution on the small curvature of certain of the particle tracks, and sufficient material in the outer layers to stop most particles and measure their energy.

A. Tracker

The track reconstruction resolves the momentum of the particle via the track curvature and also indicates whether that particle originated directly from the collision point or from a particle decay immediately thereafter. Tracking layers detect where and when particles traversed with a very high resolution, but the dynamic range of individual channels does not need to be very high. The tracker needs to be as light as possible to minimize the probability to scatter the particles. This puts a limit on the power consumption, as the material in the detector is often dominated by the cables bringing the electric power in and the cooling infrastructure removing the generated heat.

Reverse biased silicon pin diode arrays implemented on high resistivity silicon depleted over the full thickness of the wafer have become the standard for the sensors in the tracker [1,2]. Charged particle traversals generate in silicon typically about 80 electron-hole pairs per micron. In the very inner layers two dimensional diode arrays are used with a granularity of about 100 x 100 μm^2, flip-chip bump-bonded to a readout chip to form pixel detectors [5]. For the outer layers one-dimensional arrays of 10-20 cm long strip-shaped diodes are used, connected by wire bonds to integrated readout circuits. Figure 4 shows the ATLAS Silicon Central Tracker as an example of how a detector covering many square meters is constructed from readout chips and 10x10 cm^2 silicon sensors. The ABCD readout chip [6] contains 128 channels of charge preamplifier, shaper filter and comparator and has been implemented in a radiation-tolerant BiCMOS technology, however most integrated circuits installed at LHC were produced in a standard 0.25 µm CMOS technology with special layout techniques to enhance the radiation tolerance [7]. The shaper filter is commonly used to optimize the signal-to-noise in a charge sensitive front end [8-10]. Every 25 ns the state of the 128 comparators is latched, but only data corresponding to interesting events selected by the trigger signal is read out.

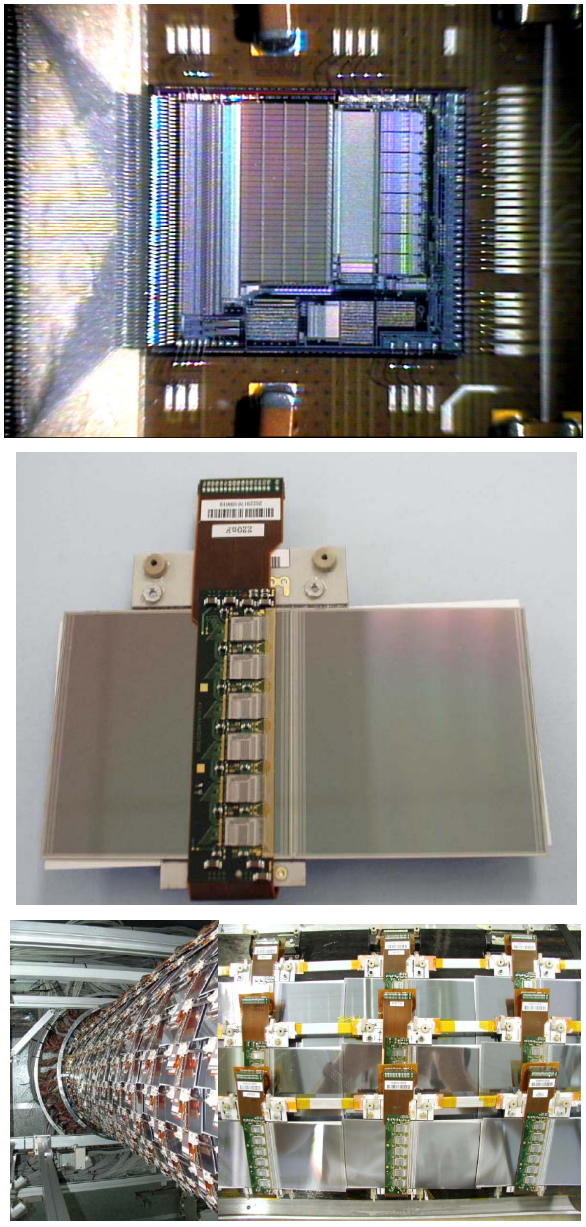

Figure 4. ATLAS silicon strip tracking detector. Top: Die picture of the ABCD readout chip used to read out 128 channels. Center: fully assembled strip detector module with 6 readout chips on one side and 6 on the other side. The strips creating the junction on one side of the wafer and the ones creating the ohmic contact on the other side of the wafer are at a slight angle with respect to each other to provide some resolution also in the direction parallel to the strips. The 20 cm long sensor is constructed from two 10x10 cm^2 dies. Bottom: detector barrel (left) and detail (right) fully assembled from these strip detector modules during system tests. © ATLAS-SCT 2015.

B. *Calorimeter*

The calorimeter provides material to absorb the particles leaving the tracker and to measure their energy over a wide range. In a homogenous calorimeter the absorber is also the sensor, as for instance in the electromagnetic calorimeter in CMS, constructed from high density (8.28 g/cm^3) scintillating $PbWO_4$ crystals, 61200 in the barrel and 14648 in the endcaps, read out by converting the generated light into an electric signal. In a heterogenous calorimeter absorber and sensor are separate, as in a sampling calorimeter alternating absorber and sensor layers. Such calorimeter can also be used to detect non-charged particles which interact in the absorber and produce showers also including charged particles which can then be detected. Hadronic calorimeters, measuring the energy of hadrons, like protons and neutrons, are typically implemented like this, with 10 to 20 layers of brass or steel layers of a few cm thick each.

The readout of calorimeters has to have a large dynamic range and uses ADCs of 12 bits or more, often preceded by a gain selection stage to optimize the ADC range to the input signal. Often but not always the ADC are commercial parts, tested to withstand the more moderate radiation levels in the outer part of the experiment.

C. *Muon detector*

Muons are very penetrating particles and are not stopped by the calorimeter. They often are the signature of interesting events and therefore a key input to the trigger selecting which events to read out. Since the muon detectors are the outemost layers of the experiment they typically need to cover very large areas, for instance about 25 000 m^2 in CMS. This is typically done using gas detectors, in which similar to silicon detectors particle traversals generate a track of ionization but now consisting of electron-ion pairs. Also here charge is collected by applying a drift field, but the amount of generated charge is typically small and therefore somewhere along the path of the electrons a high field region is created where charge is amplified by avalanche multiplication. These high field regions can be obtained around a wire by applying the positive voltage to this wire of controlled diameter such that the multiplication occurs as the electrons approach the wire. Gas Electron Multiplier or GEM detectors [11] are an alternative, where the high field region is created in holes in thin foils which have to be traversed by the electrons.

An important issue with gas detectors is that breakdowns in the gas occur relatively regularly, generating a temporary conductive path between electrodes, discharging the electrodes. If one of the electrodes is charge collection electrode connected to the input of the readout circuit, the discharge of the other electrode biased at typically 1kV with a capacitance of a few nF represents a significant charge. Protection circuitry is therefore mandatory, most of the time still implemented with discrete electronics, although sometimes it is integrated with the readout circuit [12].

IV. FUTURE CHALLENGES AND TRENDS

Power consumption, radiation tolerance and data rates are important constraints for particle physics experiments, most aggressive for the inner layers where particle fluxes are highest, and where material has to be reduced to minimize particle scattering. The number of collisions will increase in future experiment upgrades with several collisions happening at the same time, therefore requiring more functionality to disentangle events, and higher radiation tolerance and data rate capability, while it would be desirable to maintain or even lower power consumption.

A. *Circuit radiation tolerance*

Already for the presently installed detectors radiation tolerance requirements are stringent: 1 MGy or 100 Mrad and 10^{15} 1 MeV neutron equivalent/cm^2 for the inner layers. For the upgrades these values will increase by at least an order of magnitude. For the majority of the presently installed detectors at LHC, sufficient radiation tolerance was achieved using special layout techniques with annular transistors and guardrings in a standard 0.25 μm technology [7]. On finer linewidth technologies special layouts are often not needed to withstand 100 Mrad or more, but for extreme doses up to 1 Grad, significant degradation of MOS transistors has been observed in some technologies [13]. MOS technologies finer than 65 nm often include a high k gate dielectric of which the radiation tolerance needs more detailed study. Depending on the technology choice, scenarios where the very inner detector layers are regularly replaced may have to be envisaged. CMOS transistors operate at the interface of the silicon and dielectric and are not very sensitive to non-ionizing particle flux which generates displacement damage in the silicon bulk knocking out atoms from their lattice position.

Apart from integrated radiation flux, also single event effects can affect integrated circuits. Single event latch up has not been observed to be a problem at LHC. Single event upset is addressed by using triplicated logic and majority voting or by Hamming encoding in memories. Some analog blocks like phase locked loops can be sensitive and have to be designed with large capacitance values on critical nodes yielding a power penalty.

B. *Sensor radiation tolerance and trends*

Guardrings are used also in silicon sensors to improve tolerance to ionizing radiation, but silicon sensors are primarily sensitive to displacement damage generating bulk defects and traps capturing the signal charge before it is collected. Some signal can be recovered by increasing the reverse bias to reduce the travel time of the signal charge and the probability for it to captured by the traps. Significant effort has been carried out by the Rose [14-15] and RD50 collaborations [16] to develop sensors able to withstand fluences of 10^{15} n_{eq}/cm^2 or more, including detailed studies on the influence of the presence of certain impurities like oxygen in the silicon. It may be necessary to decrease the sensor thickness for the extreme radiation levels in future upgrades to continue to exploit the sensor at reasonable biases.

The availability of CMOS processes on higher resistivity substrates or epitaxial layers, for instance for imaging or high voltage applications, has raised significant interest, e.g. in ATLAS [17], not because the thickness of the sensitive layer would be reduced but to significantly reduce the sensor cost. Part of the readout circuitry can also be integrated.

Further cost and material reduction can be achieved if the readout is fully integrated with the sensor as in monolithic active pixels, or MAPS. They have been installed for the vertex tracker of STAR [18], and have been adopted for the Inner Tracker System (ITS) upgrade of the ALICE experiment at CERN, where it is planned to fully replace the present ITS in 2019 with a new 10 m^2 tracker entirely constructed using MAPS [19]. Figure 5 shows a die picture of the first full-scale prototype, which has been proven to satisfy ALICE specifications [20]. Radiation tolerance requirements in ALICE are moderate and full depletion of the sensitive layer would be needed to enhance tolerance to non-ionizing radiation beyond 10^{14} n_{eq}/cm^2.

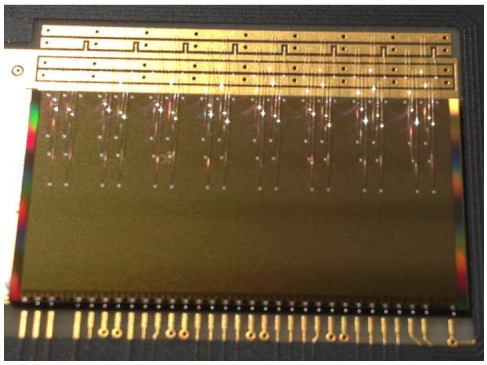

Figure 5. Die picture of the first large scale prototype for the ALICE ITS upgrade. The chip measures 3 cm by 1.53 cm and contains ~500 000 pixels. The chip is intended for flip-chip bump-bonding on a carrier, but has been wire-bonded for the first tests.

Excellent radiation tolerance of sensors in CMOS technologies has been achieved [21]. It still is a challenge, but significant work is being done for MAPS, e.g. [22-23], to combine full depletion of the sensitive layer essential for radiation tolerance, with integration of full CMOS within the pixel and a small low capacitance charge collection electrode important for low analog power consumption. Advanced integration techniques using Through Silicon Vias and similar techniques would provide an alternative to integrate sensor with readout. It is likely that significant progress in the coming years in these areas will cause monolithic detectors or advanced hybrid detectors to be more widely adopted in high energy physics experiments, providing lower cost and better performance through higher granularity.

C. *Power consumption*

If power consumption is not reduced, part of the performance advantage offered by higher granularity of MAPS or advanced hybrid detectors will be offset by the excess of material in the detector. Already now tracking resolution is scattering-dominated for all but the very high momentum particles.

The analog power consumption is dominated by the Q/C ratio or the ratio of the collected charge for a particle traversal over the capacitance at the input of the readout circuit [24,25]. The ALICE prototype of figure 5 reaches a Q/C of 80 mV distributed over a few pixels, allowing the implementation of a front end consuming only 40nW per pixel. A Q/C of 300-400mV is maybe not fully out of reach by concentrating more charge on a single pixel and further optimizing the capacitance, and this would be sufficient for a particle traversal to turn on a transistor which is off in standby, practically fully eliminating analog power.

Work on readout architectures is required to also reduce the digital power to extract the hit information from the pixel matrix and take advantage of the reduction in the analog power. The present trend in hybrid pixel detectors is to choose a fine linewidth CMOS technology for the readout chip to integrate a maximum of functionality in each pixel [5], but some alternatives with simple readout circuits in the pixel have been considered [26]. Distributing the clock to every pixel will have to be avoided for pixel sizes below 20 by 20 μm^2.

Ultimately data has to be transmitted off-chip and off-detector. Due to redundancy and increased capacitance on critical nodes to protect against single event effects, power consumption in data transmission units including PLL, serializer and driver in high energy physics remains well above 10 mW/Gb/s [27-28]. Hopefully this can be improved to approach a few mW/Gb/s reached for some other applications [29].

V. Conclusions

Integrated circuits and silicon sensors are essential in high energy physics experiments to deal with the data rates and the complexity of the produced events, also for the recent discovery of the Higgs boson. They are likely to meet the challenges for future detector upgrades regarding radiation tolerance and data rates, but continued work on optimizing power consumption is essential. Standard CMOS processes are now also being considered to implement the silicon sensor at lower cost and integrate part or the full readout circuit with it. Therefore the role of silicon and CMOS fabrication processes for use in these experiments can only further increase.

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