Comparison of Li-ion Active Cell Balancing Methods Replacing Passive Cell Balancer

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Abstract – **This article describes possible proposals of the active battery cell balancer for Li-ion battery-pack which should be used as a replacement of the common passive cell balancer in the existing battery management system. The main goal of this paper is to compare the most efficient solutions especially in terms of number of used components, size and price.**

Keywords- BMS, balancer, equalizeur, battery management, Li-io, ATA6870n

I. INTRODUCTION

Each multi-cell battery-pack consists of individual cells connected in parallel to achieve the required capacity and current and in series to achieve the required voltage. Such battery-pack should be composed of cells from the same manufacturer and production lot to ensure their parameters most consistent as possible. Even in such multi-cell battery-pack is very improbable to find just two absolutely identical cells. There are always slight differences in the state of charge, capacity, impedance and temperature dependencies. Unfortunately these differences don't stay the same but generally increase over battery life-time. This behaviour subsequently leads to the cell voltage imbalance. Cell balancing circuit (also cell equalization circuit) can significantly eliminate this behaviour, resulting in improved efficiency as well as increased overall capacity and lifetime of the battery-pack.

There are two types of balancing: active and passive. Passive method is based on the switchable resistors discharging the corresponding cell. The discharged energy is dissipated as heat. The active method employs inductors, transformers or capacitors to transfer the energy form the more charged cells to the less charged cells or between individual cells and whole battery pack. This method uses principles of the switching power supplies and is much more efficient. The capacitive method is suitable for smaller balancing currents not exceeding 100mA. The main problem of this method is that significant energy losses occur during capacitors charging, resulting in maximal efficiency of this process up to 50%. Another problem is that high voltage differences between the unbalanced cells exist only in highly discharged state. Because this method transfer rate is proportional to voltage differences, it only becomes efficient near the end of discharge so total amount of unbalance that can be removed during one cycle is low. Inductor based method allows much higher currents, typically several amperes and the balancing is independent of the cell voltages.

The purpose of the proposed cell balancers is to replace the passive balancer by the active one in the existing battery management system (BMS) [1]. Each BMS consists of one main-board and six sub-packs. Each sub-pack contains a small board (sub BMS - SBMS) (figure 1) for individual cell voltage measurement, temperature measurement and cell balancing based on the ATA6870n [2] daisy chainable circuits. Each ATA6870n allows measuring 4 - 6 cells, up to four temperatures and allows current bypassing of each measured cell by a parallel connected resistor with maximum balancing current of 100mA.

This SBMS manages 14S battery-pack (14 cells in series) via three ATA6870n. All ATA6870n communicate via vertical SPI bus among themselves and the lowest one allows communication with main board via optically isolated SPI bus. The supply voltage of the board is generated also by the internal circuits of the ATA6870n and it can be enabled or disabled by the main board also via optically isolated input.

One of the biggest problem of the current solution is the generated heat during charging caused by a high charging current and also by the passive cell balance circuit especially in case of using of the newly developed 600W fast-charger. The temperature of the cells mustn't exceed 45°C during charging to avoid permanent damage or even explosion of the cells. Because it was necessary to charge the battery as fast as possible, the mechanical design was adjusted for better performance of the active cooler allowing air flow around all cells. Electrical design of the pack was also improved to reduce the power loses by decreasing of all resistances along the current way. Unfortunately the power heating of the cells can't be reduce so the next logical step is to eliminate the additional power loses caused by the passive balancer by replacing it for an active one.

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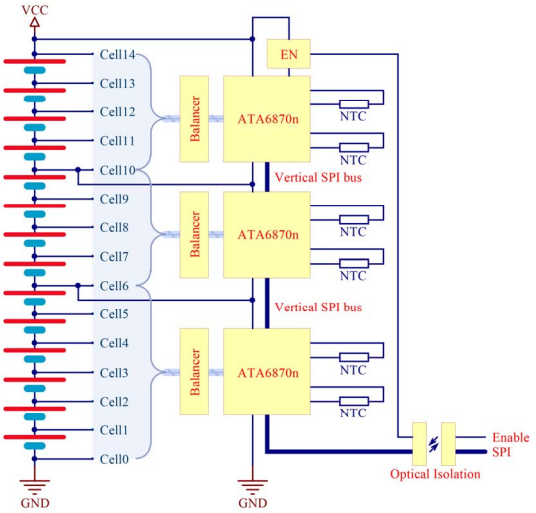

Figure 1. Block diagram of SBMS

Various kind of equalization techniques have been proposed, demonstrated, and implemented and many of them have one of the following major drawbacks. The first is a complex circuitry and control because of high switch count and the second is design difficulty and poor modularity because of the need for a multi-winding transformer that imposes strict parameter matching among multiple secondary windings or high amount of the inductors or transformers. Both drawbacks negatively influence primarily PCB dimensions and a price. In the following chapters only methods suitably applicable to the circuit ATA6870n meeting following requirements will be discussed. The cell balance current should be about 1A, proposed solution must take almost same place as the current one and the additional cost must be of course as low as possible. Due to the required balance currents and higher efficiency only inductive methods will be discussed.

II. CONSIDERED SOLUTIONS

A. *Atmel recommended design – buck-boost converter design [3]*

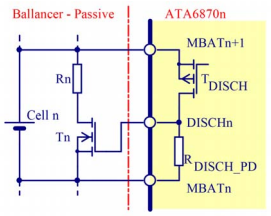

Figure 2. ATA6870n internal DISCHn control

Figure 2 shows the internal circuitry of one of six channels of the ATA6870n. DISCHn pin is normally used to drive an external discharge NMOS transistor. The pull-down resistor RDISCH_PD ensures the default low level of the pin and also prevents a parasitic cross conduction current flow when the ATA6870n is switched off. Internal PMOS transistor TDISCH pulls the pin to high and switches the external transistor via a typical output current of 1mA. The state of the internal transistor is controlled by SPI with maximum clock frequency of 250 kHz resulting in the maximum switching frequency of 3 kHz. An external parallel resistor RPD is necessary to achieve adequate switching times.

The principle of this active cell equalizer is based on the buck-boost topology allowing the energy transfer in both directions between adjacent cells in a stack [4]. It means from the cell to be discharged to the higher or lower neighbor. The problem of this topology is the requirement of two independent switches per cell but ATA6870n has only one. The solution is to replace one transistors for a diode as shown in figure 3. Then extra energy can be transferred only in one direction from a cell to its lower neighbor. This solution presents modular concept that can be used for all cells in a stack. One module generally consists of one switching PMOS transistor one diode and one inductor.

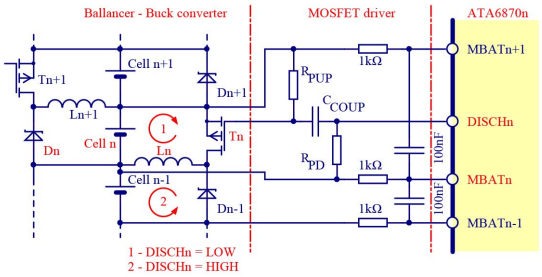

Figure 3. Energy transfer to lower neighbor cell

As described above, the switching frequency is generated in a software way by cyclic set and reset appropriate bit of the cell balance drive register in ATA6870n via SPI. After defining of the cell to be discharged on the corresponding output DISCHn is generated clock frequency of maximum 3 kHz.

When the output DISCHn is in a low level (loop 1), the PMOS transistor Tn is switched on and energy of the Cell n is transferred to the inductor Ln (see Figure 3). When the output level of the DISCHn control signal is switched to high (loop 2), the switching transistor Tn is off and the current flowing through the inductor Ln continues through the diode Dn-1 transferring the energy accumulated in the inductor Ln to the lower battery cell. The energy is transferred with only slight power losses caused by the inductor series resistance, the PMOS transistor ON state resistance and voltage drop on the diode.

This circuit allows to transfer the charge from all cells of a stack to their lower neighbor cells. However, if the lowest cell needs to be discharged, the energy has to be transferred to the highest cell of a stack to close the transfer loop. The only way is to replace the first inductor, corresponding with the first cell, for a transformer that allows to charge the highest cell of a stack (cell n), as shown in figure 4.

Figure 3 also depicts the circuit of the driver between ATA6870n output DISCHn and gate of the external transistor. The driver employs AC coupling created by the capacitor C_{COUP} to ensure short switching time of the external transistor. An

additional resistor R_{PUP} helps to guarantee that transistor is switched off safely. As mentioned above, the external resistor R_{PD} is recommended in parallel to DISCHn to achieve shorter switching times.

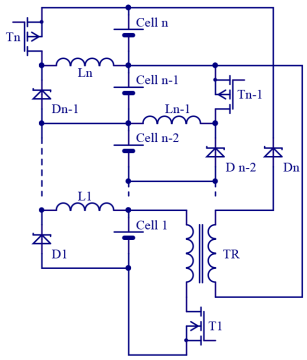

Figure 4. Transfer coupling between lowest and highest cells

Between main disadvantages of this concept belongs the low achieved frequency of maximum 3 kHz resulting in relatively large and expensive inductors for a considered equalization current. Also the number of inductors (n-1) and one transformer makes this concept more expensive. This circuit is suitable and efficient for balancing of cells lying close to each other in a stack. If the two cells that need to be balanced are separated by a long distance (Cell 1 and Cell n for instance), it would take more than one step to balance them what causes a decrease of efficiency and it will also need a longer time to transfer energy between these two cells.

The benefit of the design is that none of the switches used in the concept have high voltage stress issue and therefore the cost is reduced.

B. Magnetic coupled buck-boost design[5]

The following concept is a combination of the previous proposal, balancer based on the multi-winding transformer [6] and bidirectional flyback converter design [7] as shown in figure 5. This balancing topology reduce the number of winding, diodes and also the cost, but full functionality of the balancer is retained. Instead of the simple inductors employs one multi-winding transformer but only with a half the number of windings. The transformer turns-ration is 1:1 for cell to cell balancing method leading to a relatively high efficiency and small transformer size.

In Figure 5 L1, L2 to Ln/2 are coupled windings and each of them is shared by pairs of cells in a string (stack). For a proper function of the design is necessary to ensure that the total number of cells (n) in a string will be even (n = 2k, k = 1, 2 …) to ensure every two cells share one winding. These two cells and shared winding (C1, C2 and L1 for instance) form a buck-boost converter similar to the previous design which allows to transfer energy between these two adjacent cells in both directions. The different situation occurs when the nonadjacent cells needs to be balanced (for example C1 and C4). Due to coupled windings the cells corresponding windings form flyback converter. It means that the energy can be easily transferred from one cell to another cell utilize principles of a buck-boost converter and a flyback converter. This approach saves time and increase transfer efficiency between nonadjacent further cells. However, the energy cannot be transferred between the same parity cells because of shared windings. For example, if the energy from cell 1 needs to be transferred to the cell 3, the energy cannot be transferred directly but two steps are necessary. The energy must be transferred from cell 1 to cell 2 at first. After that it is possible to transfer the energy from the cell 2 to the cell 3.

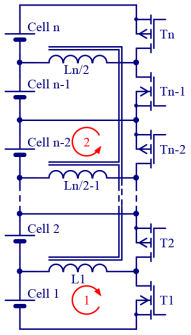

Figure 5. Magnetic coupled buck-boost converter

The proposed cell balancer can be connected to the same driver as previous design as shown in figure 3. The only difference is that this topology uses the PMOS transistors for odd number of cells and NMOS for even number of cells.

The principle is also almost same with the previous design, see figure 5. When the transistor T1 is switched on, the energy is transferred from the corresponding Cell 1 to the winding L1 (loop 1). When the T1 is switched off and the dead-time interval passed the switch Tn-2 is switched on (loop 2). The energy stored in the transformer is transferred from the winding Ln/2-1 to the corresponding Cell n-2. The dead-time interval is used to avoid the two switches being switched on the same time.

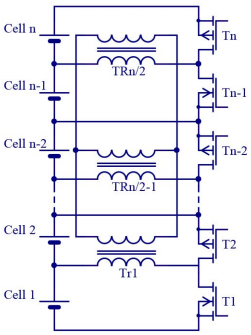

Figure 6. Secondary winding coupled buck-boost converter

Similarly to the previous design none of the transistors suffer high voltage stress what reduces the cost when compared with multi-winding transformer design. The biggest handicap of the proposed topology is the multi-winding transformer which

causes bad modularity. Solution of the problem would be replacement of the problematic multi-winding transformer for a multi transformer design with parallel interconnection of secondary windings as shown in figure 6. Also it is possible to use more multi-winding transformers with a lower number of windings for better modularity and interconnect them with help of the next winding similarly to the depicted topology in figure 6. It means a combination of both approaches.

C. *Voltage multiplier based design [8]*

This type of balancer is not based on the previously mentioned methods and also does not require high amount of switches, winding, transformers and complex switching control proportional to the number of cells. The only thing to be controlled is a turning on or off. This kind of equalizer is composed of two parts, conventional converter and voltage multiplier as shown in Figure 7. In this case the half-bridge resonant converter is used, but any other type of isolated converter can be used. The most important part is a voltage multiplier where the cells are replaced by capacitors C1' – C4'. Such voltage multiplier can produce four times higher voltage than on the capacitors C1' – C4' than the amplitude of the input voltage. In a steady condition the voltages of capacitors C1' – C4' automatically becomes uniform as the amplitude of the input signal when the diode voltage drops are neglected.

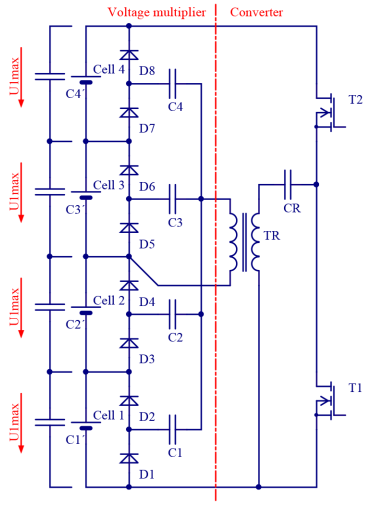

Figure 7. Voltage multiplier based design

This design requires only two switches and one diode and hence the size and cost of the circuit can be significantly reduced. It also can be designed without a multi-winding transformer and the number of series connected cells can be easily extended by adding one capacitor and two diodes per cell to the voltage multiplier and thus offer very good modularity. The only disadvantage can be an impossibility to control the balancing process by a software because this method balances fully automatically through a hardware and the only thing witch can be controlled is turning on or off the balancer. This can be a problem in a case of implementation of more complex and advanced control algorithms.

III. CONCLUSION

Due to still growing interest about using a lithium based cells in applications where it is necessary to ensure much higher voltage than one cell voltage the cells must be connected to the large series connected stacks or strings. Cell voltage balancers are necessary to ensure high reliability over years of operation and also maximize available capacity. Many types of the balancers was proposed, described, implemented but the requirements of high amount of switches, inductors, transformers or multi-winding transformers and other key and expensive components as well as the complex control methods leading to the significant design difficulty, poor modularity and high cost. The aim of this paper was described and compare only such methods witch are suitable for cooperation with ATA6870n in a cost sensitive application. Each of the described methods has own advantages and disadvantages and the choice of the specific method depends on the personal preferences.

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