Single-Phase Synchronization for Traction Active Rectifier

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***Abstract* – This paper introduces the advanced synchronization method second order general integrator phase locked loop modified especially for voltage synchronization exclusively for traction active rectifier. Designed synchronization is characterized by resistance to interfaces and especially quick response to frequency fluctuations. The behavior of designed synchronization method was analyzed by simulations tests and the final synchronization adjustment was suggested.**

Keywords- SOGI-PLL; active rectifier; single-phase; synchronization

I. INTRODUCTION

The general topology of locomotive or suburban unit is depicted in Figure 1. The electrical equipment is composed of input transformer, single-phase voltage-source active rectifier, three-phase traction inverter and traction motor. The active rectifier provides precise and fast control of dc-link voltage, proper current limitation and ensuring of harmonic trolley wire current. To ensure those active rectifier essential characteristics must be used accurate and rapid voltage synchronization method. We are talking about single-phase synchronization method, some advanced synchronization methods are presented in [1] - [10]. The main problems of single-phase voltage synchronization which are possible must be suppressed. We suppose the problem of interference during voltage measurement. Another problematic condition can be rapid changes in voltage magnitude (step changes may occur). There may be a small change in frequency (assumption is ± 2Hz), this is a slow change. Step changes in the position of the voltage vector are not expected.

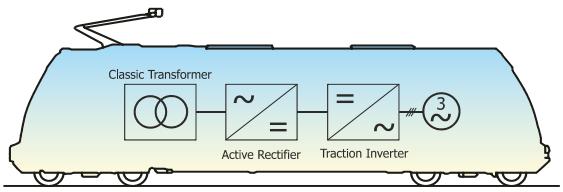

Figure 1. General topology of classic locomotive or suburban unit

II. SINGLE-PHASE VOLTAGE SYNCHRONIZATION

In the case of the three-phase supply systems are known robust synchronization voltage method. A very popular method is Second Order General Integrator Phase Locked Loop (SOGI-PLL), because there is measured only grid voltage and we obtain three information about the position of the voltage vector ϑ, magnitude of the voltage vector U_m, and fundamental frequency of voltage ω. Advantages of SOGI-PLL are simple implementation, fast response and especially sufficient resistance against distorted signal.

The block diagram of proposed single-phase SOGI-PLL synchronization is shown in Figure 2. The interference resistance of synchronization is provided by integral blocks with output signals u_α, u_β. It is based on the transfer function PI controller (1) and suitable wiring connection is possible use imaginary parts of voltage in stationary reference frame (u_β). These signal u_β and real part of voltage in stationary reference frame (u_α) are used for calculation of voltage magnitude U_m according to equation (2). The proportional controller with gain K_{SOGI} has impact to PLL signals stabilization time. At the output part is used conventional PLL structure with Park's transformation where the signals (u_α, u_β) transform from stationary reference frame to d,q rotating system, by equation (3) and (4). The better representation of this transformation is illustrated at vector diagram in Figure 3.

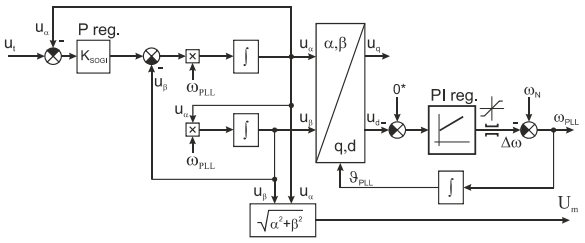

Figure 2. Single-phase SOGI-PLL synchronization

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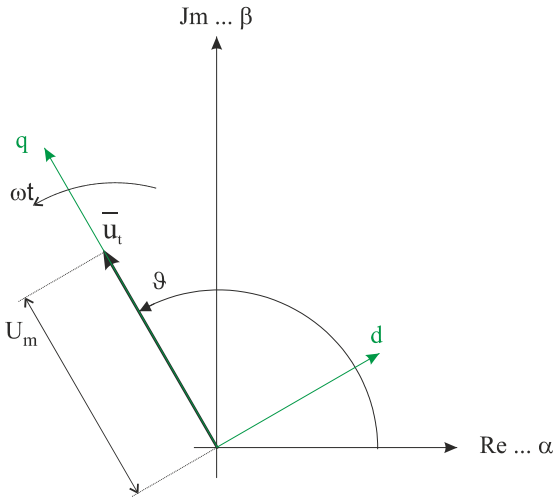

Figure 3. Vector diagram for single-phase voltage synchronization

$$F(s) = K_P . \frac{1 + \frac{K_P}{K_I}.s}{\frac{K_P}{K_I}.s} \quad (1)$$

$$U_m = \sqrt{u_\alpha^2 + u_\beta^2} \quad (2)$$

$$u_q = u_\alpha . \cos(\vartheta_{PLL}) + u_\beta . \sin(\vartheta_{PLL}) \quad (3)$$

$$u_d = u_\beta . \cos(\vartheta_{PLL}) + u_\alpha . \sin(\vartheta_{PLL}) \quad (4)$$

The PI controller (PI reg.) provides control of the reactive component of voltage (u_d) to zero value. The controller output is correction signal $\Delta\omega$, this signal speed up (eventually speeds down) angular velocity of rotating system d,q. The rotation speed of virtual rotation system d,q depends on resulting angular velocity ω_{PLL}. The PI reg. is realized by conventional PI controller with symmetrical saturation limiter. This limiter value is set to ±2 Hz (±12.57 rad.s^{-1}), because the maximal range of supply voltage frequency is expected from 48Hz to 52Hz. The maximum rate of change in voltage frequency is expected about 1 Hz/s.

The resulting angular velocity is ω_{PLL}, that we get sum of correction signal $\Delta\omega$ and nominal value ω_N. The position of voltage vector (ϑ_{PLL}) is calculated by using of integral block for the signal ω_{PLL}.

III. SINGLE-PHASE SOGI-PLL SIMULATION TESTS

The behavior of single-phase voltage synchronization is tested on developed simulation model. This simulation model is realized in C language. The simulation step is chosen with regard to the accuracy of simulation h=1^{-7} s and discrete sampling step is selected with regard to real implementation at DSP (T_{vz} = 50 µs, that is also used as relevant transport delay).

A. *Synchronization hooking*

The single-phase SOGI-PLL voltage synchronization was first tested at the starting hooking. In this case, there was only a short change at the output frequency ω_{PLL}. The stabilization time is shorter than 0.4 s in detail Figure 4.

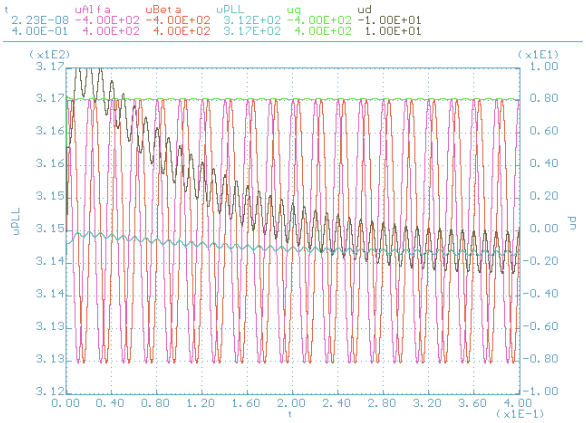

Figure 4. SOGI-PLL synchronization hooking
u_α – real votage component (80V/div), u_β – imaginary voltage component (80V/div), ω_{PLL} – PLL angular velocity (0.5rad.s^{-1}/div), uq –active voltage component (80V/div), ud – reactive voltage component (2V/dílek)

B. *Voltage magnitude changes*

The problematic condition for voltage synchronization can be rapid changes in voltage magnitude. This types of changes are caused by rapid load up or load down of supply network. The response of tested synchronization is very fast as documented in Figure 5.

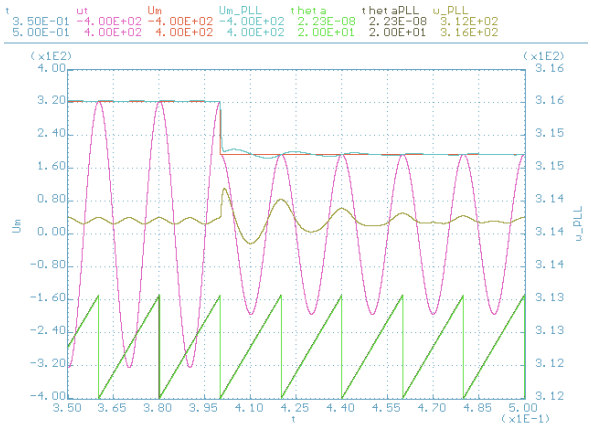

Figure 5. SOGI-PLL synchronization response to voltage change u_t – voltage input signal (80V/div), U_m – magnitude of input voltage (80V/div), U_{m_PLL} – PLL voltage magnitude (80V/div), theta – position of input voltage (2rad/div), $theta_{PLL}$ – PLL voltage position (2rad/div), ω_{PLL} – reactive voltage component (0.4rad.s^{-1}/div)

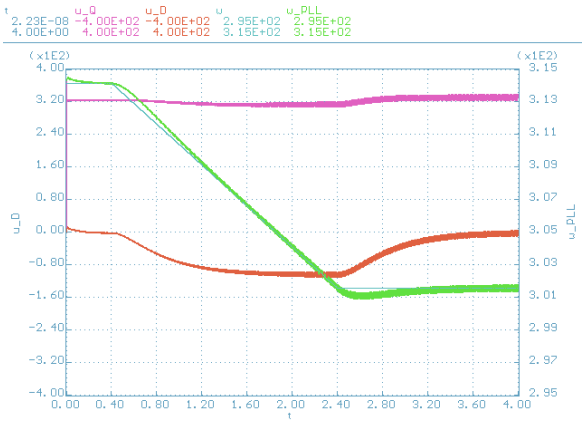

Figure 7. SOGI-PLL synchronization response to frequency change (rapid frequency change from 50 Hz to 48 Hz) u_Q –active voltage component (80V/div), u_D –reactive voltage component (80V/div), ω – input voltage angular velocity (2rad.s^{-1}/div), ω_{PLL} – PLL angular velocity (2rad.s^{-1}/div)

C. *Voltage frequency changes*

The very unpleasant condition for voltage synchronization can be changes in voltage frequency. This types of changes are also caused by high load up or load down at the supply network. The response of tested synchronization is satisfactory for step change as a shown in Figure 6. The stabilization time is shorter than 1 s during change of voltage frequency from 50 Hz to 48 Hz.

The relevant change of voltage frequency is shown in Figure 7. This frequency change is from 50 Hz to 48 Hz with rate 1Hz/s.

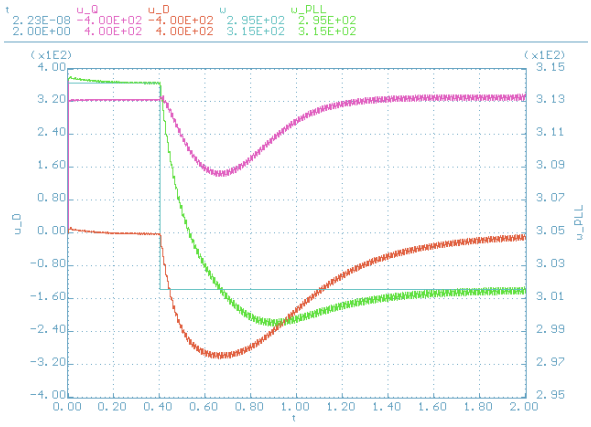

Figure 6. SOGI-PLL synchronization response to frequency change (step frequency change from 50 Hz to 48 Hz) u_Q –active voltage component (80V/div), u_D –reactive voltage component (80V/div), ω – input voltage angular velocity (2rad.s^{-1}/div), ω_{PLL} – PLL angular velocity (2rad.s^{-1}/div)

D. *Voltage position changes*

The changes in the position of the voltage vector are very problematic for PLL types of synchronization. In this case the SOGI-PLL voltage synchronization was tested for step change in position with value $\pi/2$. This test result is documented in Figure 8. and in detail Figure 9. The stabilization time is shorter than 0.5 s, but this type of change is not expected.

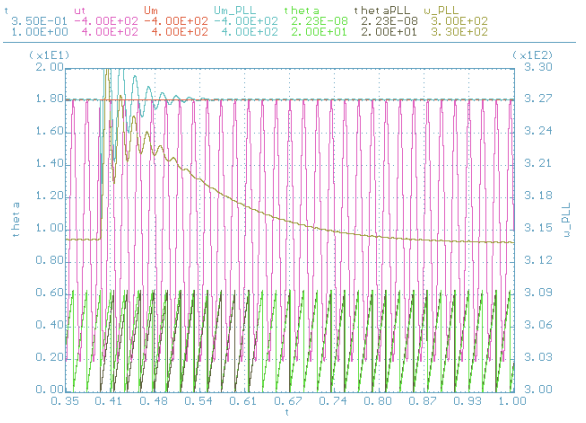

Figure 8. SOGI-PLL synchronization response to voltage position change (step change with value $\pi/2$) u_t – voltage input signal (80V/div), U_m – magnitude of input voltage (80V/div), U_{m_PLL} – PLL voltage magnitude (80V/div), theta – position of input voltage (2rad/div), $theta_{PLL}$ – PLL voltage position (2rad/div), ω_{PLL} – reactive voltage component (0.4rad.s^{-1}/div)

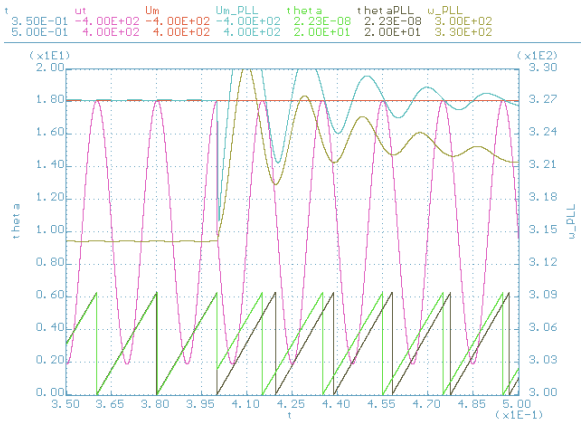

Figure 9. SOGI-PLL synchronization response to voltage position change in detail (step change with value $\pi/2$)
u_t – voltage input signal (80V/div), U_m – magnitude of input voltage (80V/div), U_{m_PLL} – PLL voltage magnitude (80V/div), theta – position of input voltage (2rad/div), $theta_{PLL}$ – PLL voltage position (2rad/div), ω_{PLL} – reactive voltage component ($0.4 rad.s^{-1}$/div)

IV. PARAMETRY SYNCHRONIZACE

The structure of presented single-phase SOGI-PLL voltage synchronization obtain two controllers. The first controller is proportional (P reg.) with gain K_{SOGI}. This gain has impact to PLL signals stabilization time and also to interference resistance. The second controller is PI (PI reg.) with K_p gain and T_i integration time constant. These constants affect the tracking speed of reactive component (u_d) and therefore voltage frequency tracking. The final controller setting was done empirically and found values are shown in TABLE I.

TABLE I. SINGLE-PHASE SOGI-PLL SYNCHRONIZATION SETTINGS

Controller label	***Controller type***	***Proportional gain***	***Integration time constant***
P reg.	proportional	$K_{SOGI}= 1$	
PI reg.	Proportional-Integration	$K_p= 0.03$	$T_i= 0.5$ s

V. CONSLUSIONS

This paper presented single-phase voltage synchronization based on SOGI-PLL structure. This type of voltage synchronization is very good solution for traction active rectifier, for example [11] - [13]. This synchronization is also suitable for use in advanced PV power station of low-power or for special single-phase power supply source [14] - [15]. The main advantage of proposed synchronization algorithm is resistance against interference and unpredictable changes in the supply voltage (magnitude and frequency). This fact was shown by the simulation behavior of SOGI-PLL.

ACKNOWLEDGMENT

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