

Study of 3.3 MW Voltage-Source Active Rectifier

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Abstract – This paper deals with the behavior and stability of three-phase voltage-source active rectifier with rated power 3.3 MW. This high-power converter is connected to power grid via transformer and input clean power filter. The main purpose of the article is check the stability of the input filter and describes harmonics spectrum at the output DC-link. For these reason, the power converter tested by accurate simulation study including the consideration of time delay of control, dead times and losing in semiconductor components.

Keywords-active rectifier; active front end; input source

I. INTRODUCTION

This paper describes the mathematical model of 3.3 MW voltage-source active rectifier (also known as an Active Front End). This model is used for testing of input power source intended to power of five special controlled converters. These electric sources are part of laboratory equipment newly established Regional Innovation Centre for Electrical engineering (RICE [1]). This mathematical model used to validate the behavior and stability of a real active rectifier which is the input part of the source laboratory. The active rectifier is powered from transformer through LC filter. This filter with transformer inductance create the clean power filter (sinus wave filter LCL type) at the active rectifier input. The total source power 3.3. MW is achieved that the source consists of three converters in parallel connection. Each of these voltage-source active rectifiers has own clean power filter (LC type) connected at input side. The output of these voltage-source active rectifiers are at output side connected to common DC-link with one large value capacitor. The topology of analyzed power source is shown in Figure 1.

The main goal is found the value of the DC-link voltage ripple at the common capacitor. The final voltage ripple frequency and harmonic component is also important with the regard to the converters connected to the output capacitor. The required value of voltage Total Harmonic Distortion (THD) is less them 5%. The most monitored frequency is 1200 Hz, with the regard to connected output converters.

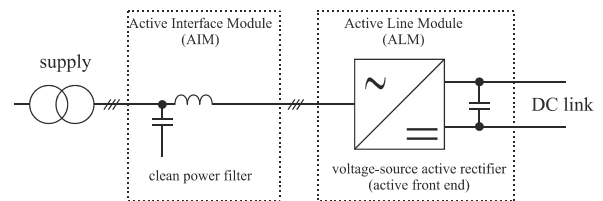


Figure 1. Simplifying topology of input source

II. SIMULATION MODEL OF POWER CONVERTER

The mathematical model was created in Matlab/Simulink/Plecs software. The simulation parameters are based on the measured values of real clean power filter, calculated values of the input transformer, converter parameters taken from the datasheet. The converter model is composed of three independent active rectifier connected in parallel as a shown in Figure 2. These active rectifier converters are modeling, including semiconductors voltage loses, dead times and time delay causing by discrete control algorithm.

The control of voltage-source active rectifiers (three parallel converters) is provided by same modulation signals. The same PWM strategy is used for active rectifiers. The designed control is based on DQ current control algorithm which is based on vector control in “virtual” revolving reference frame linked to a space vector of grid voltage. A dc-link voltage controller is realized as a conventional PI controller and commands the magnitude of required active component of trolley-wire current. The reactive current component is control to zero value. The complete control algorithm of voltage source active rectifiers is shown in Figure 3. The detail description included mathematical theory is possible to find in [2] - [4] The parameters of simulation are in detail listed in TABLE I.

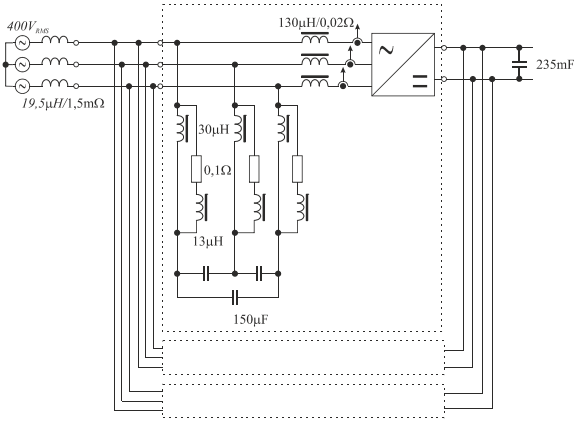


Figure 2. Diagram of three-phase voltage-source active rectifier mathematical model

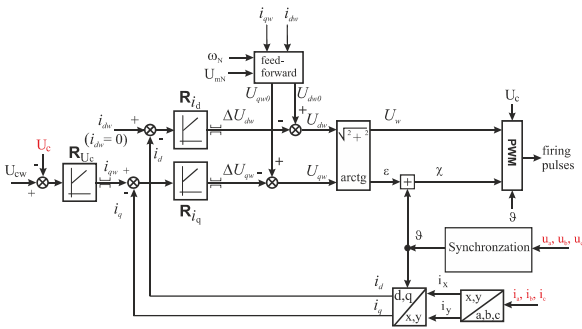


Figure 3. Vector control in virtual reference frame used for control of three-phase voltage-source active rectifier

TABLE I. PARAMETERS OF THREE-PHASE VOLTAGE-SOURCE ACTIVE RECTIFIER MATHEMATICAL MODEL

Description	Label	Value
Voltage of supply transformer	u_a, u_b, u_c	400 $V_{RMS}/50$ Hz
Induction of supply transformer	L_{TR}	19.5 μH
Parasitic resistance of of supply transformer	R_{TR}	1.5 $m\Omega$
Switching frequency of active rectifier	f_{switch}	1250 Hz
Dead time duration of active rectifier	t_{dt}	3 μs
Total capacity of output DC-link capacitor	C_{DC}	235 m F
Capacity of filtering capacitor (LC)	C_{LCL}	150 μF
First inductor of LC filter	L_{p1}	30 μH
Parasitic resistance of L_{p1}	R_{p1}	5 $m\Omega$
Second inductor of LC filter	L_{p2}	13 μH
Parasitic resistance of L_{p2}	R_{p2}	100 $m\Omega$
Converter side inductor of LC filter	L_{conv}	130 μH
Parasitic resistance of L_{conv}	R_{conv}	20 $m\Omega$
Required voltage value at output DC-link	U_{dcw}	1030 V

III. SIMULATION RESULTS

The behavior of 3.3 MW Voltage-Source Active Rectifier is tested on developed simulation model. This simulation model is realized in Matlab/Simulink/Plecs. The model is realized including transistors dead times delay and with consideration to discrete sampling time. The accurate model is closer to reality and brings the impact to current harmonic content [5]. The sampling time is selected with regard to real implementation ($T_{PWM} = 1/1250$ s, that is also used as relevant transport delay). In Figure 4. is shown active rectifier currents with source voltage during steady stay for nominal power 3.3 MW. The resulting harmonic analysis of these currents is depicted in Figure 5. The controlled voltage U_{DC} is pure as shown in Figure 6. The resulting harmonic analysis of output voltage is depicted in Figure 7. The harmonic spectrum distribution corresponds to the basic theories listed in [6] - [8]. The current ripple and the resulting voltage ripple depends on proportional gain of PI controller. When the proportional gain increasing (approximately 10x) the voltage ripple raise as a shown in Figure 8. and harmonic analysis in Figure 9.

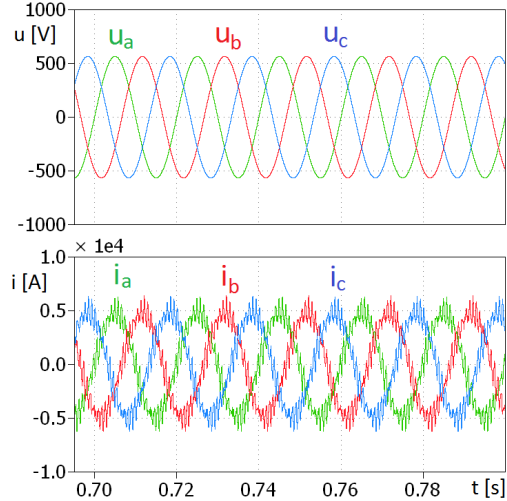


Figure 4. Phase currents and voltages for converter under steady-state condition (load power $P=3.3MW$)

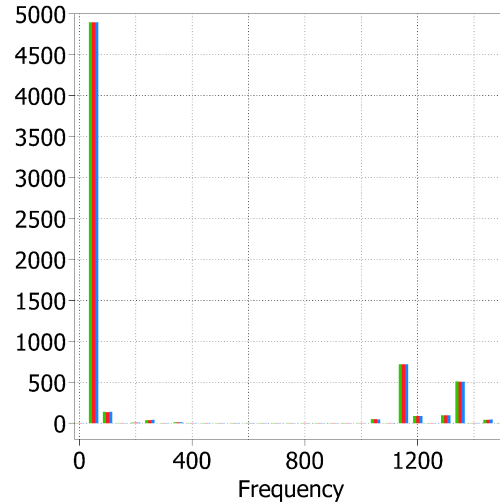


Figure 5. Harmonic analysis of the phase currents under steady-state condition (load power $P=3.3MW$)

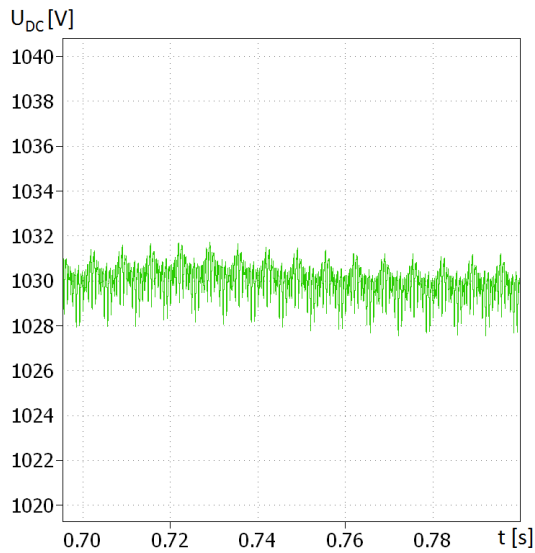


Figure 6. The voltage waveform at the common DC-link under steady-state condition (load power $P=3.3\text{MW}$)

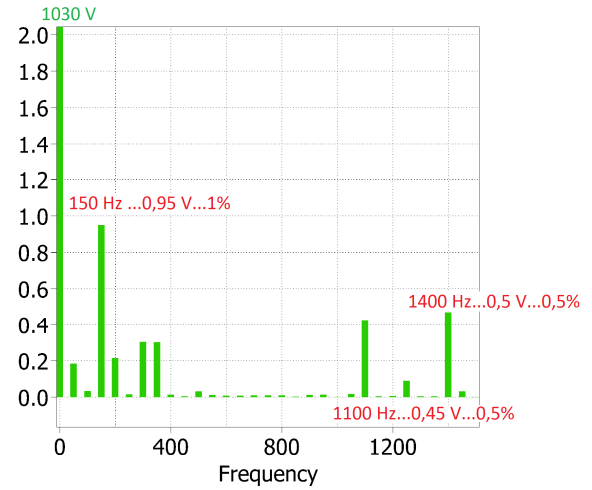


Figure 9. Harmonic analysis of the voltage at common DC-link under steady-state condition (load power $P=3.3\text{MW}$, for the high proportional gain)

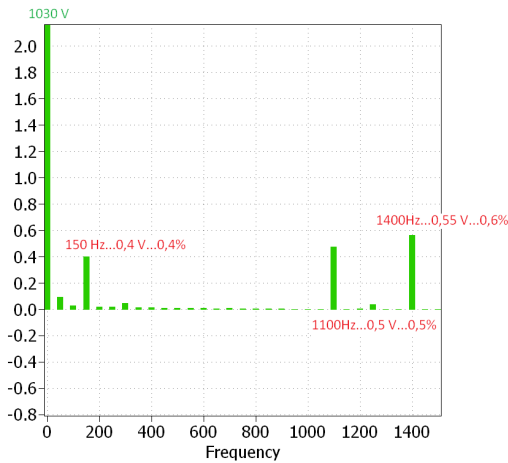


Figure 7. Harmonic analysis of the voltage at common DC-link under steady-state condition (load power $P=3.3\text{MW}$)

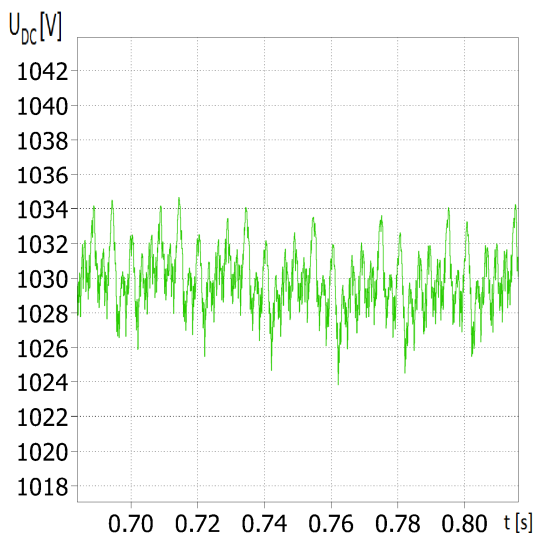


Figure 8. The voltage waveform at the common DC-link under steady-state condition (load power $P=3.3\text{MW}$, for the high proportional gain)

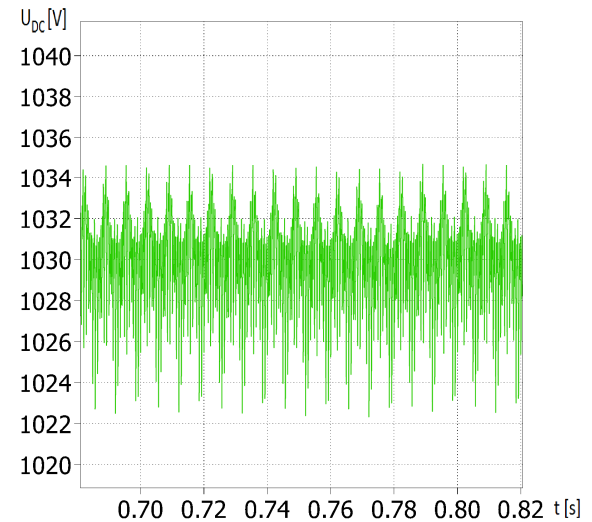


Figure 10. The voltage waveform at the common DC-link under steady-state condition (load power $P=3.3\text{MW}$, for the $C_{DC}=72\text{mF}$)

During load disconnection, the resulting capacity is reduced to 72mF (output inverters with DC links capacitors part are disconnected). The main impact is possible seen in Figure 11. , the final harmonics analysis is different.

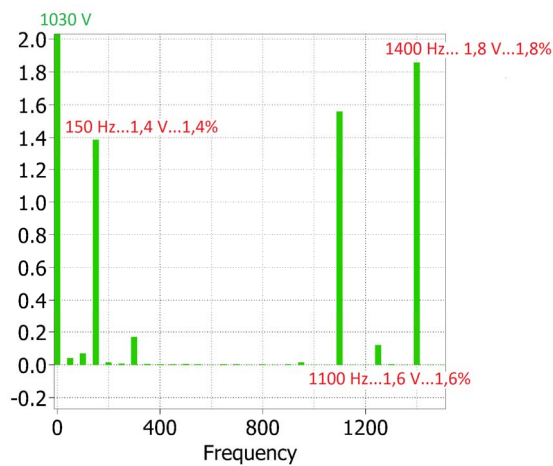


Figure 11. Harmonic analysis of the voltage at common DC-link under steady-state condition (load power $P=3.3\text{MW}$, for the $C_{DC}=72\text{mF}$)

IV. CLEAN POWER FILTER

The correctly designed clean power filter provides sinusoidal current without ripple on output side (grid side). In this case the simulation result show that the output current (grid side) is rippled like the input current (converter side) Figure 12. In this case the clean power filter is not well selected as a evidenced by bode diagram in Figure 13.

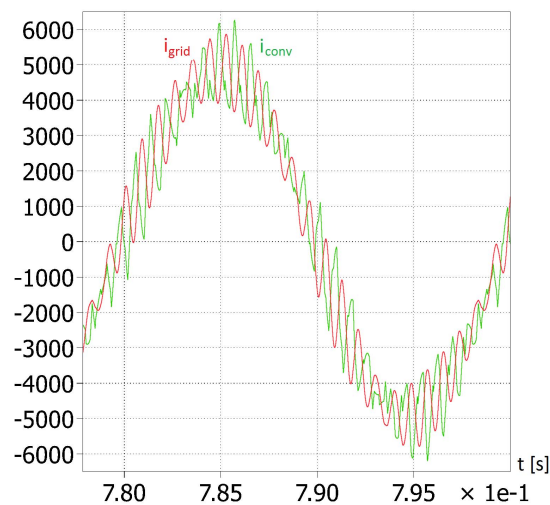


Figure 12. Currents in detail (load power $P=3.3\text{MW}$)

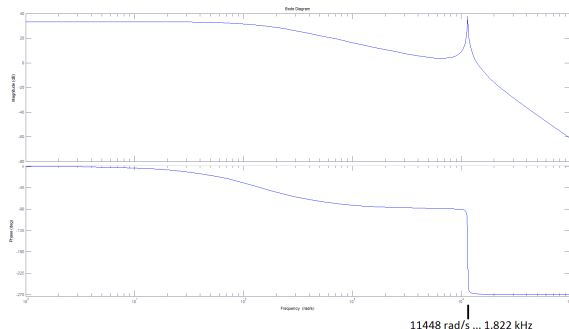


Figure 13. Bode diagram of LCL filter

V. CONCLUSIONS

This paper presented simulation results of three-phase voltage-source active rectifier with rated power 3.3 MW. This electric source is part of laboratory equipment for newly established Regional Innovation Centre for Electrical engineering. The important monitored parameter voltage ripple at common DC-link has value 4 V as presented in Figure 6. The problematic voltage harmonics are possible to found at frequency 1100 Hz and 1400 Hz as seen from the results of harmonic analysis Figure 7.

The designed clean power filter unable eliminate current distortion from converter side Figure 12.

ACKNOWLEDGMENT

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