Design aspects of the SC circuits and analysis of the cross–coupled charge pump

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***Abstract*—This paper presents some real properties of the cross-coupled charge pump that is used in low-power microelectronic integrated systems operating with high voltage (FLASH, EEPROM memories). SC-circuits characterization and design aspects are firstly discussed. Theoretical analysis of the cross-coupled charge pump with accompanying equations has been done. Some real properties have been simulated by ELDO Spice and compared with these assumptions. Simulation results show discrepancy between calculation and simulated parameters due to significant pumping losses that have been discussed in detail. Discontinuity of the output voltage through input parameters is very important finding that complicates the development of the real model for design purposes.**

Keywords - SC circuits, description, cross-coupled charge pump, simulation, pumping losses, discontinuity.

I. INTRODUCTION

Discrete-time analog circuits (DtAC) have been developed since the second half of the 20th century. DtAC have been divided into two main groups according to the principle of the function as a result of the microelectronic technology development. Switched–capacitors circuits (SC) were firstly implemented in the early 80´s and switched–current circuits (SI) up in the 80´s of the 20th century [1]. The second mentioned group is still in the growth.

These systems are characterized by analog switches representing a nonlinear component, thus DtAC are generally *nonlinear systems*. Attention will be focused on SC circuits with an external clock signal input designed for signal applications (the sampling theorem must be generally respected). Currently, SC circuits represent very perspective sector of quasi–analog systems. Options of the unipolar monolitic technology solve the basic problem associated with the integration of precise and stable resistor networks. The basic principle is based on the resistor simulated by the switched-capacitor C [3]:

$$R_{ekv} = \frac{T_c}{C} = \frac{1}{f_c C}, \tag{1}$$

where $f_c = 1/T_c$ is the clock signal frequency.

SC circuits are mainly used for the implementation of active filters–ARC structures. There are also special applications in an analog domain including integrated voltage converters–*charge pumps*. Charge pumps are circuits that use switched-capacitors as an energy storage elements to convert (decrease, increase or invert) input voltage without using of the inductors. These blocks have become an important part of low-power circuits operating with high input voltage [8] (FLASH, EEPROM memories, etc.).

This paper deals with specific type of the charge pump–*the cross-coupled charge pump*. Detailed analysis have not been published yet, thus design aspects and general description of SC circuits will be firstly explained. The main part includes both the theoretical analysis accompanied by equations and simulation of real properties in the professional design environment Mentor Graphics with evaluation of the achieved results.

II. SC CIRCUITS DESCRIPTION

DtAC design represents the fundamental problem, which relates to the solution of the part steps of the design algorithm. The following three key steps are necessary for successful proposal: *circuit model, simulation* and *evaluation of the simulation results*. These are closed associated with the general description, as will be discussed bellow. Simulation must be exclusively done in *transient analysis*. Calculation is long–time process due to many iterations to achieve of the optimal solution. Feedback correction of the model is very useful for this purposes. Characterization system

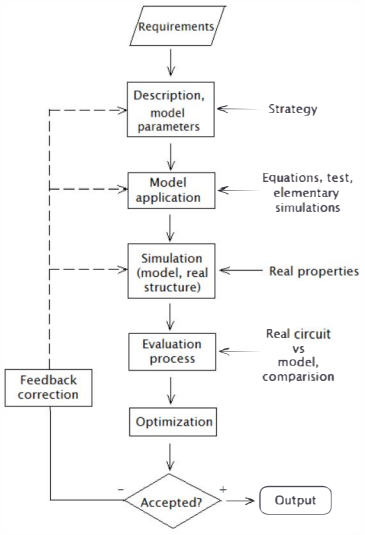

Fig. 1. Design algorithm of the DtAC.

has been published in many books and research papers

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([1], [2], [3]). However, universal design process has not been known. Quasi–analog systems take over some characteristics of the analog circuits and others from the digital circuits. Some important characteristics are summarized in table I. Two logical approaches exists to

TABLE I
SOME PROPERTIES OF DTAC

Analog systems	Digital systems
form of processed signal	signal processing in D.t.
frequency limitation	clock signal
dynamic properties	ambiguous properties
environmental influence	easy tunnable
(temperature)	(filters)
reproducibility	easy integration

the problem of the description: continuos and discrete-time signal processing. First approach assumes that the DtAc behaves as an analog circuit. The system is described by the differential equations for each phase of the clock signal supplemented by the initial conditions. This method is complex but the computational algorithms are very difficult. Moreover, the transition into the frequecy domain often requires special form of the circuit functions. The second aproach neglects continuous signal in time and system is described in the steady state as a digital circuit. Equations can be directly assembled in the frequency domain (Z–transform) [2].This access is very simple compared with the first method but the process leads to the *ideal case*. Needless to say, inclusion of the real parameters into the calculation in discrete-time is *limited to the mathematical tools to express transfer function* in the Z–transform. More information and desciption methods are reported in [2].

III. CROSS-COUPLED CHARGE PUMP (CTS-2)

Cross coupled charge pump in Fig. 2 is based on the principle of Dickson´s charge pump. N–stage architecture ([7], [9]) is additionally supplemented by the switches (transistors M_{S1}–M_{SN}) in order to eliminate threshold voltage of the diodes realized by MOSFET transistors M_{D1}–M_{DN} (CTS-1 architecture [9]). It allows to achieve higher efficiency. Two–phase clock signal ϕ and $\bar{\phi}$ controlls transport charge between main capacitors C_i. Switch transistor in each

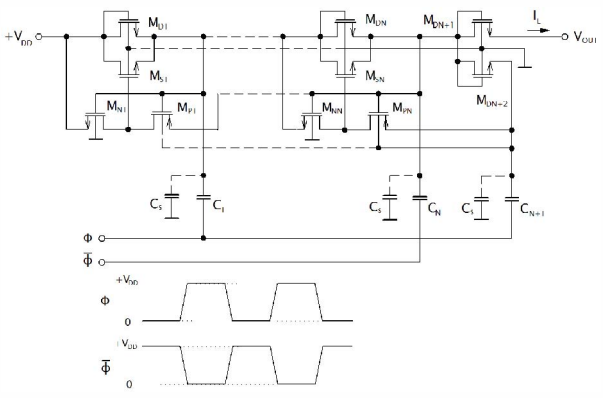


Fig. 2. Cross-coupled charge pump.

stage is controlled by the output signal of the inverter (M_{Ni}, M_{Pi}) that is supplied by higher voltage from the next stage (feedback signal). The control circuit ensures that switches will be turned on/off in the time intervals defined by logic levels of the clock signal.

The maximal output voltage is theoretically given by

$$V_M = (N+1)V_{DD} - V_{THM_{DN+1}}, \tag{2}$$

where N is number of stages, V_{DD} is supply voltage and $V_{THM_{DN+1}}$ is threshold voltage of the transistor $M_{D_{N+1}}$. Average value of the output voltage on the resistive load, labeled R_L, is derived from SC technique (Eq. 1):

$$V_{out,av} = V_M - \frac{N}{f_c C} I_L = \frac{V_M}{1 + \frac{N}{fCR_L}}, \tag{3}$$

where I_L is average value of the load current.

Required number of stages to achieve a desired output voltage is characterized by pump´s voltage efficiency η_v[1],

$$\eta_v = \frac{V_{out,av}}{(N+1)V_{DD}}. \tag{4}$$

IV. ANALYSIS OF REAL PROPERTIES

Some real properties of the charge pump will be discussed and shown in the simulation results in this section. Charge pump has been tested by the professional simulator ELDO Spice including real models of the components (library MGC Design Kit). Static and dynamic parameters were simulated for the specific parameters that are (unless noticed otherwise) given in Table II. The elementary simulation of the output voltage in steady state was performed in the first instance and compared with the known theoretical solution from the previous. The table III lists the average output voltage vs. number of stages, the percent error ε_{Vout} between the calculated (Eq. 3) and the measured value of $V_{out,av}$ and pump´s voltage efficiency η_v. Analysis results show definitely mismatch between measured and calculated values due to description of the ideal case.

TABLE II
SIMULATION PARAMETERS

Parameter		Value
Number of stages	N	2
Supply voltage	V_{DD}	1V
CLK frequency	f_c	10MHz
Main capacitance	C	5pF
Load ressistance	R_L	100k
Load capacitance	C_L	10pF
Threshold voltage of	V_{TH0_N}	0.35V
NMOS and PMOS at V=0	$\lvert V_{TH0_P}\rvert$	0.33V
Channel length of N(P)MOS	L	1μm
W/L ratio of the M_{Si}	W_s/L_s	2
M_{Pi}	W_p/L_p	3
M_{Ni}	W_n/L_n	1
M_{Di}	W_d/L_d	25

There are many reasons, why the transport charge is lossy. The losses can be devided into two main groups:

[1]Voltage efficiency ignores power consumption, as is apparent from definition of it. Real energy efficiency is allways less than η_v.

TABLE III
STATIC AND DYNAMIC PARAMETERS OF THE CHARGE PUMP

N[-]	$U_{out,ov}$[V]	$\varepsilon_{rV_{out}}$[%]	η_v[%]
1	1.12	32.5	56
2	1.54	17.9	51.3
3	1.89	14.86	47.25
4	2.19	12.4	43.8
5	2.41	11.4	40.17

static and dynamic losses. First, dynamic losses are caused by the capacitive coupling between stages (charge injection). These occur during fast changes in time, typically during rising and falling edge of the clock signal. Dynamic losses depend on the frequency and affect total current consumption.

Second, static losses decrease voltage at each of nodes, thus limit output voltage. Strange capacitance [8] connected to each of the nodes (see Fig. 2) is significant component of the static losses because it creats the voltage divider with main capacitance, $V_{DD}^{'} = V_{DD}\frac{C}{C+C_s}$. Strange capacitances can be interpreted by the parasitic capacitance of the MOSFETs and layout capacitances [8].

Threshold voltage is a critical parameter, because it represents potential barrier for input voltage. A sufficiently high voltage must be applied to gate of the switch transistor M_{Si} to suppression of the threshold voltage of the transistor M_{Di}. It means, the voltage gain ΔV of the stage must be greater then

$$\Delta V > \frac{V_{TH}}{2} \tag{5}$$

for the correct function. *Provided the condition (5) is not satisfied, the circuit operation is the same as Dickson´s charge pump*. Therefore, the function of the output voltage and efficiency have discontinuities, as is shown in Fig. 4 and 6. Unfortunately, potential barrier is supported by the different bias voltage on the bulk and source electrods of MOSFETs (Body effect). The relationship between the source-bulk voltage and threshold voltage is given by the simplified following equation for *long channel* MOSFET ([4], [5], [6], [8]):

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\phi_s - V_{SB}} - \sqrt{\phi_s}\right), \tag{6}$$

where V_{TH0} is threshold voltage at zero bias voltages, ϕ_s is surface potential and γ is body effect coefficient (calculated from the model parameters).

This circuit eliminates reverse charge transport during the phase of the CLK *more* than the previous version CTS-1 [9]. However, this problem still exists in the actual version (see Fig. 3). Reverse transport

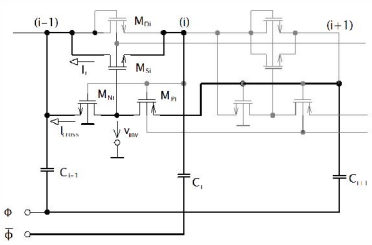
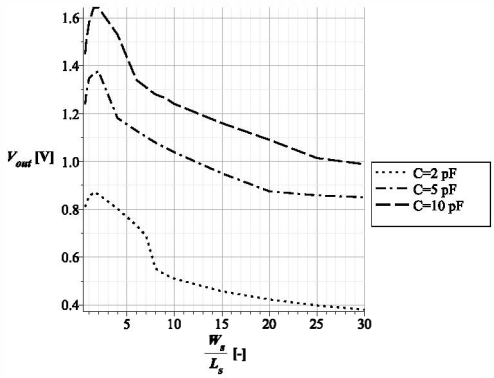
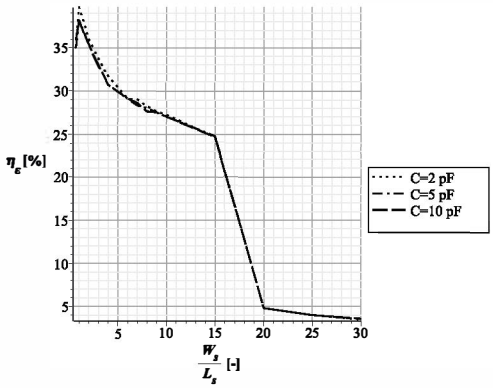


Fig. 3. Reverse transport charge.

charge is caused by the *reverse current of the switch transistor* I_r and *the inverter´s cross current* I_{cross}. Both the current loops are higlighted in Fig. 3. Reverse current is carried out, if the immediate reverse voltage gain $\Delta V_r > 0$ and $V_{inv} - V_{(i-1)} > V_{THMsi}$. Implying that, disproportionately large ratio W_s/L_s of the switch transistor greatly decreases the output voltage. There is the optimal point in the characteristics (see Fig. 4), in which the *output voltage* (Fig. 4a) and *pump´s efficiency* (Fig. 4b) come up to the maximum value. It is very important knowledge for the practical design. Power efficiency as the dynamic parameter is



(a)



(b)

Fig. 4. Output voltage (a) and power efficiency (b) vs. W_s/L_s ratio and the main capacity as the parameter.

determinated by the mean output power P_{out} divided by the total mean input power P_{in} in steady state (when the average value of the output voltage and current will be constant with time).

$$\eta_\varepsilon = 100 \cdot \frac{P_{out}}{P_{in}} = 100 \cdot \frac{P_{out}}{P_\phi + P_{\bar{\phi}} + P_{V_{DD}}}, \tag{7}$$

where $P_\phi + P_{\bar{\phi}}$ is total mean power supported by the clock signal generator and $P_{V_{DD}}$ is mean power supported by the DC source voltage.

CMOS inverter [4] should switch on the transistor M_{Si} during charging of the main capacitor and switch off it during charge transport into the next stage. However, inverter behaves as an analog block despite its primary function in the circuit. Output voltage of the inverter v_{inv} may be in undefined state from the view of logic levels. It means, the operating point is located in the linear part of the transfer voltage characteristics and the cross current flows through both the transistors

M_{Pi} and M_{Ni}. Inverter´s cross current is maximal at point $v_i = v_{inv}$. This point is called inverter switching point V_{SP} [4], see Fig. 5. Derivation of V_{SP} will be

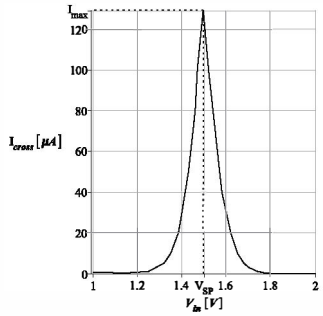


Fig. 5. Inverter´s cross current characteristics.

found based on the fact that the drain current of each MOSFET operating in the saturation region must be equal [4]:

$$\frac{\beta_N}{2\alpha_N}(V_{GS_N} - V_{THN})^2 = \frac{\beta_P}{2\alpha_P}(V_{SG_P} - |V_{THP}|)^2, \quad (8)$$

where β is the current factor, α is the modulation factor [6] and $V_{GS_N} = V_{SP} - V_{(i-1)}$, $V_{SG_P} = V_{(i+1)} - V_{SP}$. Thence,

$$V_{SP} = \frac{V_{(i+1)} - |V_{THP}| + \sqrt{\frac{\alpha_P}{\alpha_N}\frac{\beta_N}{\beta_P}}\left[V_{(i-1)} + V_{THN}\right]}{1 + \sqrt{\frac{\alpha_P}{\alpha_N}\frac{\beta_N}{\beta_P}}}. \quad (9)$$

Inverter switching point is setting both the value of the cross current I_{cross} and the *reverse current* I_r. The relationship between both the parameters is obvious because $I_{cross} = \mathrm{f}(V_{SP})$ and $I_r = \mathrm{f}(V_{inv})$. Voltage range of the *transition part of the inverter´s output voltage characteristics* $v_{inv} = f\left(v_{(i)}\right)$ *including* V_{SP} *is a critical parameter.*

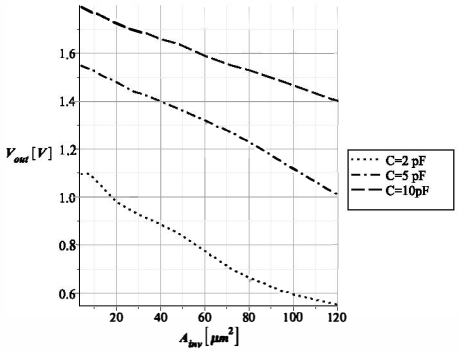


Fig. 6. Pump´s output voltage vs. total inverter area for $R = 1/3$ and $W_s/L_s = 2$.

Thus, dependence of the pump´s output voltage on the cross current (via sizing of the transitors M_{Pi} and M_{Si}, see Fig. 6) should be analyzed respecting the following conditions because of the objective evaluation:

- Reverse current must be suprresed as much as possible, so that the ratio W_s/L_s is set to the point, in which the output voltage is maximal (see Fig. 4).
- Reverse control voltage (v_{inv}) of the switch transistor should be remain the same with increasing the ratio W_{Ni}/L_{Ni} and W_{Pi}/L_{Pi} (V_{SP} = constant.). It means, the absolute ratio $R_{inv} = \frac{W_{Ni}}{L_{Ni}}/\frac{W_{Pi}}{L_{Pi}}$ must be also constant, as follows from Eq. 9.

The *inverter area* A_{inv} from Fig. 6 is given by

$$A_{inv} = W_{Ni}L_{Ni} + W_{Pi}L_{Pi}. \quad (10)$$

V. Conclusion

General characterization of SC circuits and some real properties of the *cross-coupled charge pump* were discussed in this paper. Design optimization is primarily based on the simulation process due to difficult or idealization description of the discrete-time analog circuits. However, the creation model including dominant real properties can significantly reduce simulation time. Atenttion was mainly focused on the theoretical and practical analysis of the cross-coupled charge pump that falls into this category. Simulation results show that pump´s output voltage decreases approximately linearly with the total inverter area, asumming the constant absolute strengths ratio both of transistors at fixed channel lengths. Output voltage is also strongly dependent on the sizing of the switch transistors due to discharge–reverse current. Ratio W/L must be designed to maximize the ratio of the charge and discharge current. The feedback loop represented by inverter can be opened due to undersized voltage gain of the stage. Hence, the system exhibits the discontinous character from the view of the output voltage and other parameters (efficiency). This is the main disadvantage of the cross-coupled charge pump, which greavly complicates the design circuit. Many real effects do not permit use the above equations for practical design.

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