Dynamic Duty-cycle Limitation of the Boost DC/DC Converter allowing Maximal Output Power Operations

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***Abstract*—This paper describes the concept of the dynamic duty-cycle limiter of the boost dc-dc converter. Duty-cycle limitation in boost converters is usually used to protect the bottom switch against an excessive current, and also to avoid instability occurring at high duty-cycle operations. Compared to fixed limitation, dynamic limiter enables to detect and maintain maximal possible output voltage V_{MAX}, when desired output voltage cannot be provided *e.g.* due to excessive load current or increased resistance of the switches. This feature allows to extend the operation range of the converter and powered device. Developed method applies to low power converters, and it is based on the power balance condition detection circuit. This detection is realized *via* simple and low consumption voltage sensing. Paper presents description of the method, circuit implementation and shows simulated results obtained with integrated 0.13µm CMOS boost dc-dc converter.**

I. Introduction

Boost converter is a non-isolated power converter that may be used when a higher output voltage than the one provided by the input source is required. It contains two power switches, one inductor and an output capacitor. For an ideal converter (R_{COIL}, R_{LOW}, and $R_{HIGH} = 0$), the output voltage can be determined by the volt-second balance as a function of the input voltage V_{IN} and duty-cycle D [1]:

$$V_{OUT} = \frac{V_{IN}}{1-D} \tag{1}$$

The inductor (or input) current can be obtained as function of the load and duty-cycle:

$$I_{COIL} = \frac{V_{IN}}{R_L(1-D)^2} = \frac{I_{OUT}}{1-D} \tag{2}$$

For ideal boost converter, a zero duty-cycle D provides $V_{OUT} = V_{IN}$, whereas for $D \to 1$ results in infinite output voltage V_{OUT}, and also infinite inductor current I_{COIL}.

Compared to ideal V_{OUT} (1), real converter produces lower output voltage for the same duty-cycle. This limitation can be demonstrated by the circuit of real boost converter *Fig. 1 a*). This converter contains inductor and switches parasitic resistances R_{COIL}, R_{BOT} and R_{HIGH}. At high output current, these resistances are responsible for dominant power loss of the converter [1].

Steady-state output voltage V_{OUT} of real boost converter can be obtained by the help of averaged model shown in *Fig. 1 b*). Here, technique of linearization [2], [4] employing controlled sources was used. DC analysis of this model allows to obtain the output voltage as:

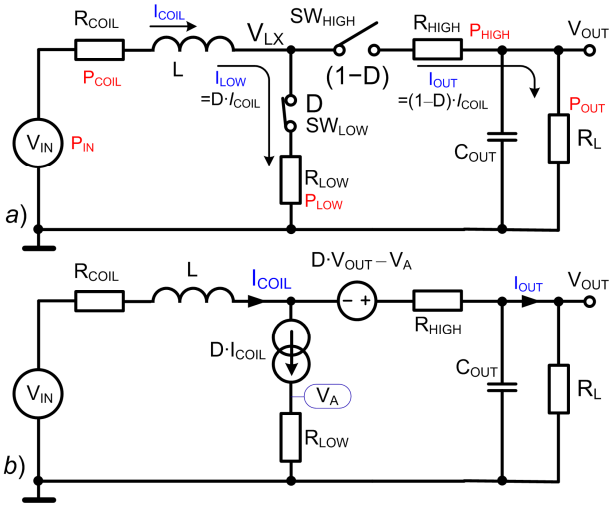

Fig. 1. a) boost dc-dc converter with dominant resistive parasitic elements [1], *b*) linearized model [2], [4].

$$V_{OUT} = \frac{R_L(1-D)V_{IN}}{D^2R_L - D(2R_L + R_{HIGH} - R_{LOW}) + R_L + R_{HIGH} + R_{COIL}} \tag{3}$$

The reduction of the output voltage is demonstrated for various load resistances R_{LOAD} in *Fig. 2*. V_{OUT}/V_{IN} conversion characteristics with $R_{LOAD} < \infty$ contains three significant areas:

1) $\boldsymbol{D < D_{CRIT}}$: normal operations with positive gain, where characteristic is close to ideal *Eq.*(1),
2) $\boldsymbol{D = D_{CRIT}}$: providing maximum output voltage V_{MAX},
3) $\boldsymbol{D > D_{CRIT}}$: negative gain area, where the output voltage decrease with increasing duty-cycle.

In normal mode of the feedback regulation, the control loop maintains the desired output voltage, and converter operates below the critical duty-cycle D_{CRIT}. However, due to *e.g.* high load current, insufficient input power, or increase of the converter switches resistance (due to the temperature increase, or by the drop of the MOSFET switch gate-source voltage), V_{OUT} can decrease below desired value (1), and the feedback loop saturates. In an extreme scenario, controller increases the duty-cycle D above D_{CRIT} and the conversion gain V_{OUT}/V_{IN} becomes negative. Beyond the loop instability, high duty-cycle operation leads to excessive inductor current (2) and potential damage of the bottom switch.

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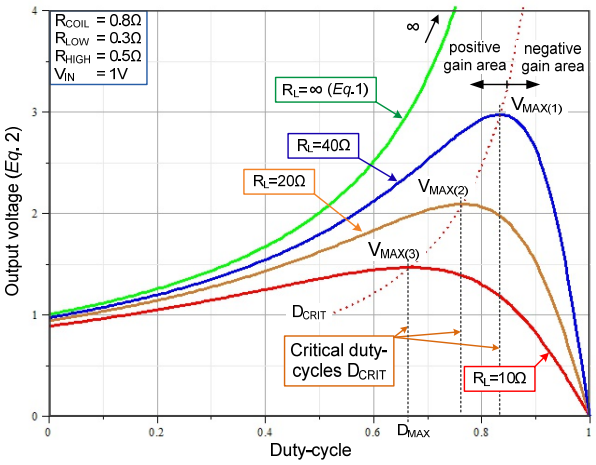

Fig. 2. V_{OUT}/V_{IN} DC voltage transfer function plotted of the real boost converter plotted by use *Eq.*(3).

The value of critical duty cycle D_{CRIT} can be obtained by setting the 1st derivative $d(V_{OUT})/dD = 0$ as:

$$D_{CRIT} = 1 - \sqrt{\left(R_{COIL} + R_{LOW}\right)/R_L} \tag{4}$$

and is independent on R_{HIGH} (R_{HIGH} can be seen as a part of the load).

In order to avoid the gain polarity inversion and also the excessive inductor current I_{COIL}, duty-cycle is usually clamped to a fixed value D_{MAX} [1], [3]. This maximal duty-cycle is designed in a way to always maintain positive conversion gain, *e.g.* $D_{MAX} < 0.67$ in *Fig. 2*. However, in normal regulation mode (where duty-cycle limitation is not required), fixed value D_{MAX} can reduce the output voltage range. As example, $D_{MAX} = 0.67$ from *Fig. 2* clamps the maximal output voltage to 2.4V when $R_{LOAD} = 40\Omega$. By setting $D_{MAX} = 0.83$, the converter can provide $V_{OUT} = 3V$ for $R_{LOAD} = 40\Omega$, or even $V_{OUT} = 5.2V$ at $R_{LOAD} = \infty$.

In this paper, concept of the dynamic duty-cycle limitation is described. Presented circuit allows to automatically determine the optimal duty-cycle D_{CRIT} for wide range of load, switch and inductor resistances. The dynamic limitation is based on the power balance concept presented in *section II*. Implementation of the critical duty-cycle detection circuit is described *in section III*, whereas feedback loop circuit allowing dynamic (real-time) limitation is described in *section IV*. This section also present results obtained by the post-layout simulations of the integrated CMOS converter.

II. Power Balance Method

In linear circuits, maximal power that can be transferred from a voltage source V_0 with output resistance R_{OUT} is obtained, when R_{OUT} is matched to the load resistance, *i.e.* $R_{OUT} = R_{LOAD}$. In this case, P_{LOSS} dissipated on the source resistance is equal to the power P_{LOAD} delivered to the load:

$$P_{LOSS} = P_{LOAD} \tag{5}$$

The output resistance R_{OUT} of the boost converter can be obtained by DC analysis of the linear model *Fig. 1 b*) described in [4]:

$$R_{OUT} = \frac{R_{COIL} + (1-D)R_{HIGH} + DR_{LOW}}{(1-D)^2} \tag{6}$$

where the output resistance increase with duty-cycle ratio. The R_{OUT} allows us to rewrite the output voltage (3) as $V_{OUT} = V_0 - R_{OUT}I_{LOAD}$. Here, V_0 corresponds to ideal output voltage (1).

As already mentioned, the maximal power transfer theorem (5) applies for linear circuits only. This signifies, that R_{OUT} (but not R_{LOAD}) should be constant, independent on the load current. However, inserting D_{CRIT} into (6), result in $R_{OUT(CRIT)}$ being a function of R_{LOAD}, and thus of the output current I_{LOAD}:

$$R_{OUT(CRIT)} = R_L + \sqrt{R_L} \cdot \frac{\left(R_{HIGH} - R_{LOW}\right)}{\sqrt{R_{COIL} + R_{LOW}}} \tag{7}$$

A condition of linearity of $R_{OUT(CRIT)}$ can be derived from equation $R_{OUT(CRIT)} = R_L$, resulting in:

$$R_{LOW} = R_{HIGH} = R_{SW} \tag{8}$$

In other words, when $R_{LOW} = R_{HIGH}$, $R_{OUT(CRIT)}$ is constant and equal to R_L. This corresponds to the condition of the impedance matching required by (5).

Fortunately, mismatch $R_{LOW} \neq R_{HIGH}$ has very low impact to the maximum power point. This low sensitivity can be demonstrated by the plot shown in *Fig. 3*. Here, relative and absolute errors of V_{OUT} and D have been plotted in wide range as function of the ration R_{HIGH}/R_{LOW}. It results, that approximate using of (5) can yield accurate optimum in a wide range of switch resistances.

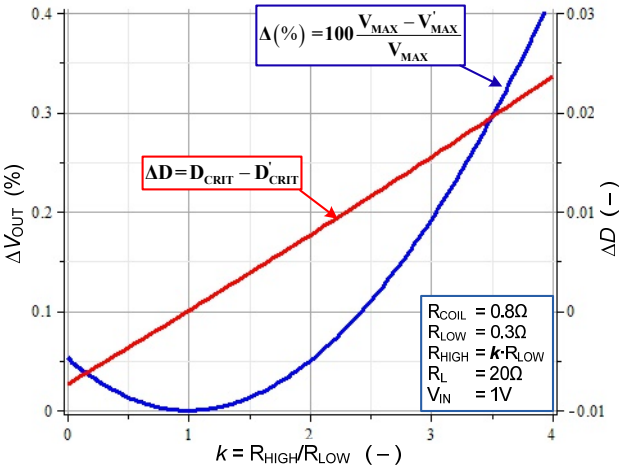

Fig. 3. Impact of mismatch $R_{LOW} \neq R_{HIGH}$. Values D_{CRIT} and V_{MAX} are obtained by using ideal D_{CRIT} (4), whereas D'_{CRIT} and V'_{MAX} from use condition (5).

It is interesting to mention, that for a converter operating at $D = D_{CRIT}$ (4), the inductor current has constant value $I_{COIL(CRIT)}$, which is independent on the load resistance R_{LOAD}:

$$I_{COIL(CRIT)} = \frac{1}{2}\frac{V_{IN}}{R_{COIL} + R_{SW}} \tag{9}$$

By regulating I_{COIL} to $I_{COIL(CRIT)}$ (*e.g. via* duty cycle or load resistance value), maximal output power operation

can be obtained. However, this regulation would requires an accurate knowledge and high time stability of R_{COIL}, R_{SW} and V_{IN}.

Next section presents an approach allowing to obtain the power balance condition (5) through simple and low consumption voltage sensing of the converter internal nodes.

III. CRITICAL DUTY-CYCLE DETECTION

In order to provide detection of the power balance condition (5), power dissipated in the converter and load resistances needs to be measured.

As shown in the converter schematic in *Fig. 1 a*), the inductor current is commutated between the low and high side switch resistances R_{LOW} and R_{HIGH} during D and $(1-D)$ fraction of the period T_{SW}. Power dissipated in the converter structure can be then written as weighted contribution of R_{LOW} and R_{HIGH}:

$$P_{LOSS} = I_{COIL}^2 \left(R_{COIL} + DR_{BOT} + (1-D) R_{UP} \right) \quad (10)$$

The entire load current I_{LOAD} is delivered through the high-side switch during $(1-D)$ portion of the period T_{SW}. Load power P_{LOAD} from (5) can be then written as:

$$P_{OUT} = I_{COIL} (1-D) V_{OUT} \quad (11)$$

Comparing P_{OUT} to (10) as required by power balance (5) results in:

$$I_{COIL} (1-D) V_{OUT} = I_{COIL}^2 \left(R_{COIL} + DR_{BOT} + (1-D) R_{UP} \right) \quad (12)$$

Advantageously, squared values of I_{COIL} can be eliminated, which allows to obtain voltage equation:

$$(1-D) V_{OUT} = \underbrace{I_{COIL} R_{COIL}}_{V_{COIL\_AVG}} + \underbrace{I_{COIL} R_{LOW} D}_{V_{RLOW\_AVG}} + \underbrace{I_{COIL} R_{HIGH} (1-D)}_{V_{RHIGH\_AVG}} \quad (13)$$

In this equation, the right side represents the sum of average voltage drops on R_{COIL}, R_{LOW}, and R_{HIGH}, whereas left side corresponds to the output voltage V_{OUT} scaled (PWM modulated) by $(1-D)$.

A. Measurement of the Average Voltages

The boost converter with RC filter voltage sensing circuits is shown in *Fig. 4*. Here, measured average voltages indicated by the arrows correspond to terms mentioned in (13).

Typically, inductor current in CCM (continuous conduction mode) converter delivering high output current contains a DC component with a small triangular ripple part. Consequently, DC voltage V_{COIL_AVG} can be obtained by filtering inductor terminal voltage. This approach is frequently used in current sensing circuits such as [6]. Voltage across RC-filter capacitor C_1 is then $V_{COIL\_AVG} = I_{COIL} \cdot R_{COIL}$. Similarly, switch voltages V_{RLOW_AVG} and V_{RHIGH_AVG} are obtained by RC low-pass filters. In particular, R_{LOW} and R_{HIGH} are conducting the current I_{COIL} during D and $(1-D)$ portion of the period, respectively. It result that V_{RLOW_AVG} and V_{RHIGH_AVG} are weighted by D and $(1-D)$ terms as intended by (13). Compared to this, term $(1-D)V_{OUT}$ is obtained by PWM modulation and filtering of the output voltage V_{OUT}, but can also be generated from V_{IN} ($V_{IN} = (1-D)V_{OUT}$).

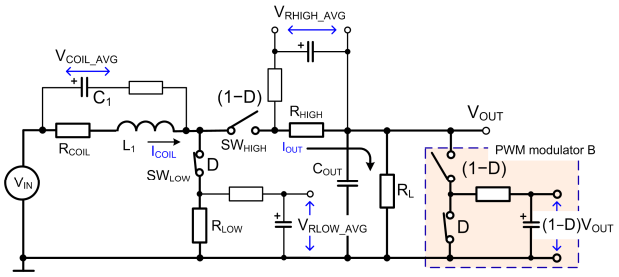

Fig. 4. Sensing circuit of voltage terms form *Eq.*(13).

In order to compare left and right side of (13), three floating voltages are to be measured and added. Ideally, this would require at least three differential high-input impedance amplifiers.

B. Modified Power Balance Sensing Circuit

In order to simplify the circuit implementation of the power balance detection, *Eq.*(13) has to be rearranged. In particular, $R_{COIL} \cdot I_{COIL}$ can be split as:

$$I_{COIL} R_{COIL} = I_{COIL} R_{COIL} D + I_{COIL} R_{COIL} (1-D) \quad (14)$$

Using this term in (13) reveals the power balance condition (5) to be:

$$(1-D) V_{OUT} = I_{COIL} \left\{ R_{COIL} D + I_{COIL} R_{COIL} (1-D) \right\} + I_{COIL} \left\{ R_{BOT} D + R_{UP} (1-D) \right\} \quad (15)$$

Here, terms with D and $(1-D)$ can be collected:

$$\underbrace{(1-D)\left(V_{OUT} - I_{COIL} R_{COIL} - I_{COIL} R_{UP} \right)}_{V_{(1-D)\_AVG}} = \underbrace{D\left(I_{COIL} R_{COIL} + I_{COIL} R_{BOT} \right)}_{V_{D\_AVG}} \quad (16)$$

This equation allows us to realize the detection of the power balance condition (5) by measuring the average voltages $V_{(1-D)\_AVG}$ and V_{D_AVG}, both referred to the ground. If $V_{(1-D)\_AVG} = V_{D\_AVG}$ converter operates at the maximum possible output voltage, *i.e.* deliver maximal output power.

Schematic realization of (16) is shown in *Fig. 5*. The operation of this circuit can be described as follows: inductor RC filter capacitor C_1 is charged to DC voltage $R_{COIL} \cdot I_{COIL}$. During the low-side switch conduction phase D, current I_{COIL} creates voltage $R_{LOW} \cdot I_{COIL}$ on the low-side switch resistance. Thanks to conducting bottom switch SW_{LOW}, C_1 positive terminal (1) is at voltage $I_{COIL}(R_{BOT} + R_{COIL})$. During this conduction phase, node (1) is connected to R_A by PWM modulator A. During

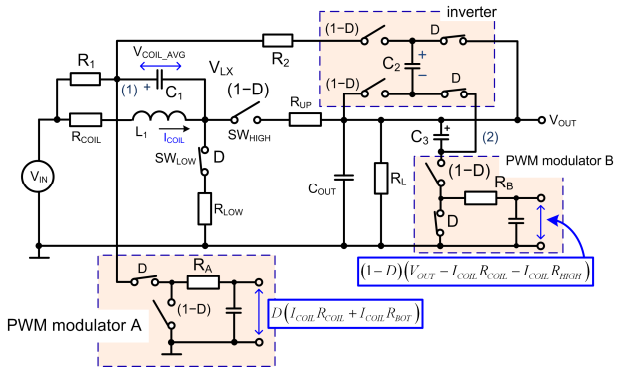

Fig. 5. Modified power-balance sensing of voltages from *Eq.*(16).

opposite conduction phase (1−D), RC filter input is connected to GND. This allows to obtain scaled DC voltage D·I_{COIL}(R_{BOT} + R_{COIL}) from right-side of (16).

Obtaining the left side of (16) is more difficult. Here, voltage I_{COIL}(R_{COIL} + R_{HIGH}) should be subtracted from V_{OUT} and weighted by (1−D) term. This subtraction is realized by an additional switched-capacitor "inverter" circuit shown in *Fig. 5*. Voltage I_{COIL}(R_{COIL} + R_{HIGH}) is generated during (1−D) conduction phase by serial connection of C_1, and voltage drop of the high-side switch voltage I_{COIL}·R_{HIGH} *via* SW_{HIGH}. Switches (1−D) related to the inverter then allow to average and store this voltage in C_2. During the complementary phase D, inverter subtracts this voltage from V_{OUT} and stores the result in C_3. Steady-state voltage of the node (2) is V_{OUT} − I_{COIL}(R_{COIL} + R_{HIGH}). Consequently, weighting by the term (1−D) is provided by PWM modulator B, and allows us to obtain the left side of (16).

Behavior of power balance sensing circuit from *Fig. 5* is shown by the switched-mode simulation in *Fig 6*. Here, we notice that V_{D_AVG} increases with increasing duty-cycle, whereas $V_{(1-D)\_AVG}$ decreases.

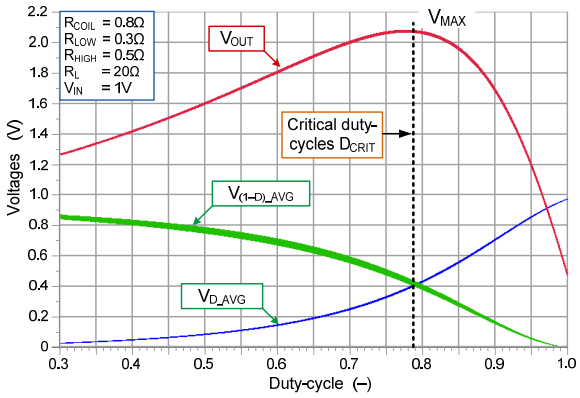

Fig. 6. Switched-mode simulation of the circuit from *Fig. 5*.

Crossing point V_{D_AVG} = $V_{(1-D)\_AVG}$ then corresponds to peak voltage V_{MAX} (maximal output power), achievable by the converter for given operating point. Moreover, difference $V_{(1-D)\_AVG}$ − V_{D_AVG} allows to determine the gain of the critical duty-cycle limitation circuit, which is suitable for the synthesis of the feedback control transfer function of D_{CRIT}.

As given by (5), operations at D = D_{CRIT} results in the power loss P_{LOSS} dissipated by the converter being equal to the power delivered to the load. As already mentioned, this limits the use of the dynamic duty-cycle limiter to the low-power converters.

IV. Dynamic Duty−cycle Limiter Feedback Loop

While the boost converter operates below critical duty-cycle D_{CRIT}, feedback control loop (current or voltage mode) maintains the regulation of V_{OUT}, and voltages $V_{(1-D)\_AVG}$ > V_{D_AVG}. By *e.g.* increasing I_{OUT}, $V_{(1-D)\_AVG}$ and V_{D_AVG} approach (see *Fig. 6*). Exceeding the critical duty-cycle D_{CRIT} results in $V_{(1-D)\_AVG}$ < V_{D_AVG} and in a decrease of V_{OUT} below required (regulated) value. In this condition, the main feedback loop saturates. However, while $V_{(1-D)\_AVG}$ < V_{D_AVG} occurs, the dynamic duty-cycle limiter takes control over the main voltage

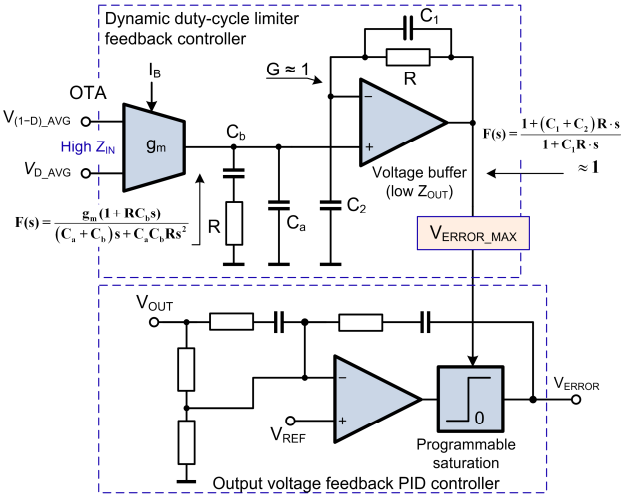

Fig. 7. OTA feedback controller [7] of dynamic duty-cycle limiter and main feedback PID controller regulating the output voltage.

regulation loop, and try to regulate $V_{(1-D)\_AVG}$ = V_{D_AVG}. This allows the converter to operate with D_{CRIT}, and maintain V_{OUT} at highest possible value V_{MAX}.

Circuit of dynamic duty-cycle limiter feedback loop is shown in *Fig. 7*. Here, we can see the main feedback loop PID controller (can be also be part of the current-mode controller), and the dynamic duty-cycle limitation circuit connected to the detection circuit from *Fig. 5*. The dynamic limitation circuit interacts with the PID controller *via* programmable saturation block. In order to protect the high-impedance voltages $V_{(1-D)\_AVG}$ and V_{D_AVG}, the duty-cycle limitation controller is realized by an OTA with very high input impedance [7]. The voltage buffer creates a low-impedance output with small derivative response, which allows to improve the speed of the duty-cycle limitation feedback loop.

The block of programmable saturation shown in *Fig. 7* is placed inside main PID controller. This allows to prevent the integrator from accumulating an input error, when the main feedback loop is saturated (anti wind-up [8]). In fact, programmable saturation block is realized by powering the last (output) stage of the PID operational amplifier by V_{ERROR_MAX}.

Operation of the dynamic duty-cycle limitation can be demonstrated by the load transient simulation shown in *Fig. 8*. Here, before applying a 6Ω load, converter operates in regulation, $V_{(1-D)\_AVG}$ > V_{D_AVG}, and V_{ERROR_MAX} is clamped to V_{OUT}. By applying R_{LOAD} = 6Ω, output voltage starts dropping below desired value, $V_{(1-D)\_AVG}$ and V_{D_AVG} approach, and PID output V_{ERROR} tries to compensate decreasing V_{OUT}. Simultaneously, V_{ERROR_MAX} decreases with V_{OUT}, until $V_{(1-D)\_AVG}$ cross V_{D_AVG}. At this time, V_{ERROR_MAX} falls below V_{OUT}, and clamps the value of V_{ERROR}. Now, regulation of the converter output voltage is provided by the dynamic duty-cycle limiter at D = D_{CRIT}, and $V_{(1-D)\_AVG}$ = V_{D_AVG}. As we can see, the converter output voltage V_{OUT} reaches highest possible value, and allows to deliver maximal output power (voltage) for given operating conditions. This is visualized in *Fig. 8* by comparison with open-loop simulation of the converter with 6Ω load, and D linearly increasing from zero to one.

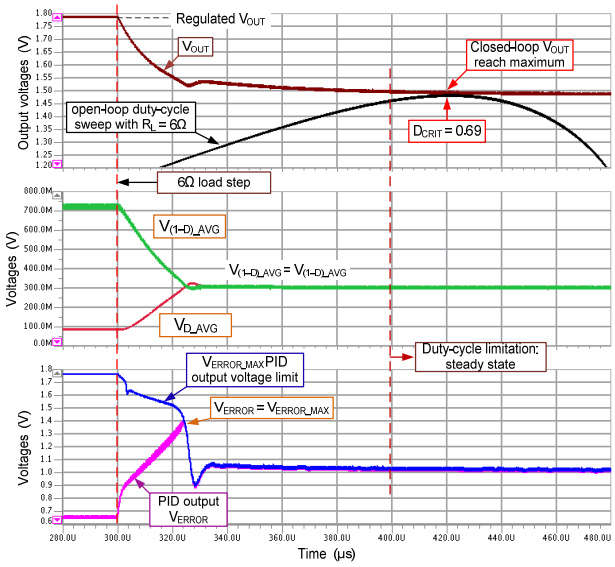

Fig. 8. Example of the post-layout simulation of the duty-cycle limitation circuit. Comparison with the open-loop duty cycle sweep allowing to verify the value of maximum output voltage V_{MAX}.

IV. Input Source Resistance Power Sensing

As given by the power balance condition (5), the power dissipated in converter must be equal to the power dissipated by the load. However, if the input source resistance R_{IN} is not negligible, it must be included in the consideration (R_{IN} and R_{COIL} are serially connected). In other word, power $R_{IN}I_{COIL}^2$ is to be added to P_{LOSS} of (5). This situation is shown in *Fig. 9*.

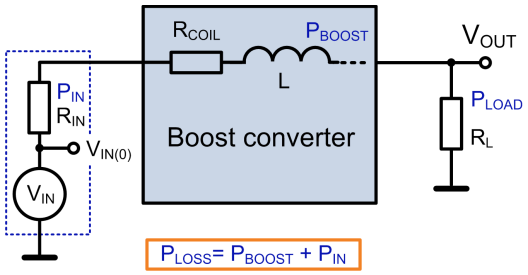

Fig. 9. Illustration of the power dissipated in the boost converter and input source resistance R_{IN}.

The difficulty of the input source resistance power sensing can occurs *e.g.* in the battery-powered converter, or converter powered by the photovoltaic cell (without MPTT – maximum power point tracking feature), where $V_{IN(0)}$ is not available.

A solution to bypass the input power sensing problem is to emulate the input source voltage $V_{IN(0)}$, and refers the inductor RC filter resistance R_1 to this voltage. This configuration is shown in *Fig. 10*. Here, an estimation of the input voltage $V_{IN(0)}$ is provided. This estimation is based on the generation of estimated voltage V_{IN_EST}. If the estimated $V_{IN(0)\_EST}$ is accurate enough, RC filter R_1C_1 measure the average voltage on the serial connection of R_{IN} and R_{COIL}.

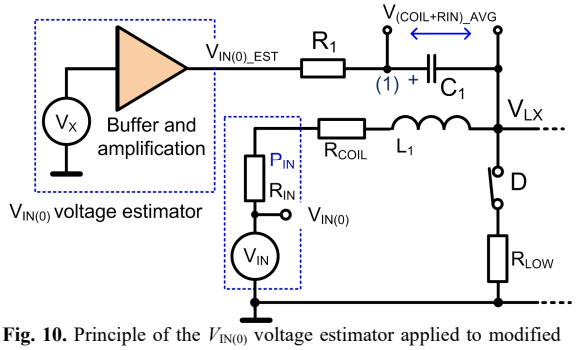

Fig. 10. Principle of the $V_{IN(0)}$ voltage estimator applied to modified power-balance sensing circuit from *Fig. 5*.

Generation of $V_{IN(0)\_EST}$ is to be based on an particular knowledge of the employed power source, and also required accuracy of the output power optimization. For instance, $V_{IN(0)\_EST}$ can be an open-ended battery voltage, open-ended voltage of an reference (small) photovoltaic panel, or it can be generated as function of environmental conditions (operation temperature, battery discharge, expected load current etc.). However, efficiency of this methodology has not been verified at the date of present paper publication.

V. Conclusion

The presented dynamic duty cycle limiter allows to maximize the output power of the boost dc-dc converter, when the main regulation loop is unable to provide desired output voltage. During this critical operation, maximization of the output power helps to guarantee the best possible biasing of the converter control circuits as well as the load. Consequently, this allows to avoid a premature circuit shoot-down, and improve optimal use of the input power source. Presented circuit was integrated in 0.13µm 5V CMOS process. Further work aims the characterization of the fabricated circuit, and focus on the optimization of the input source internal resistance power loss sensing.

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