Experimental Ripple Suppression Performance of a Virtual Infinite Capacitor

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***Abstract*—We experimentally show the performance of a Virtual Infinite Capacitor (VIC) in suppressing the voltage ripple. VIC mainly uses a bi-directional DC-DC converter with only two small capacitors inside to mimic the filtering process of a large capacitor by applying suitable control algorithms. It was firstly proposed in [1], [2] and then improved in [3] in both control algorithms and circuit designs. Based on VIC's control algorithm in [3], we injected the DC voltage together with a 50Hz, 85V (peak-to-peak) sinusoidal ripple to the VIC, and we achieved outstanding filtering performance in both the simulation and experiment. The 85V voltage ripple is eliminated and the DC voltage is extracted with no visible 50Hz ripples.**

I. Introduction

Large filtering capacitors are commonly used in industries, such as maintaining the internal voltages of submodules in a modular multilevel converter (MMC) at constant level, connection between two back-to-back voltage source converter (VSC) from the PV solar arrays to the grid, etc. They are also installed in some consumer electronic devices e.g. flat screen TVs. Even the common applications such as smoothing the output voltage of a power factor compensator (PFC) requires a bulky capacitor at its output terminal.

The concept of VIC was firstly proposed in [1] [2], aiming to use a bidirectional converter, which is defined as a canonical switching cell in [4], to smooth the low frequency ripples. Very similar circuits have been used for power filtering (without introducing the VIC concept) in [5], [6], [7] and a less similar but still related circuit appears in [8]. Also, different alternative circuits to smooth the voltage have been proposed, see (in chronological order) [9], [5], [6], [10], [11], [12], [7], [1], [2], [8] and the references therein. But VIC can eliminate random voltage ripples, making no priori assumptions about the internal models.

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We modified VIC in both control algorithm and circuit design in [3], and achieved better filtering performance, lower switching frequency, and lower power loss, which laid the foundation for the hardware implementations of VIC. This modified VIC has been tested by simulations in the applications of PFC [3] and MMC [13]. The modified circuit is shown in Fig. 1, where q, $\tilde{q}$ are binary signals to control two MOSFETs.

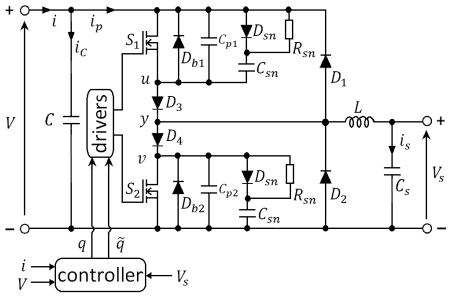

Fig. 1. The modified realization of the VIC.

In this paper, the experiment is conducted to verify the performance of VIC in large ripple suppression based on the design and control algorithm in [3]. An auto-transformer, which is to generate the sinusoidal ripples, is connected in series with a DC voltage supply, and directly injected to the VIC, aiming to control the voltage to its reference without ripples. The ripple suppression performance in experiment will be compared to that in simulation.

VIC is a nonlinear capacitor, with the Q-V characteristics as shown in Fig. 2. There are three stages, which are power up, VIC normal operation (flat region), and overcharging stage which needs to be avoided by some protection methods. The VIC controller is to ensure the VIC behave as Fig.2, among which only the normal operation stage is what we are actually interested

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in. An additional control mechanism called 'charge control' is required to maintain the VIC staying in this stage [1] [2] [13] [3]. However, in this paper, we only aim to demonstrate the performance of VIC controller and thus ignored this charge control for simplicity. Thence, we are able to see the clear transition between two neighboring stages periodically. And, totally four situations are presented in the experiment, that is, the power up process, power up & normal operation process, normal operation process, normal operation & protection process. Amongst these situations, the normal operation process can only last for a few seconds owing to the lack of 'charge control', but it is enough for us to check VIC's voltage filtering performance. This is a very straightforward way to verify the filtering ability of the VIC without any interference.

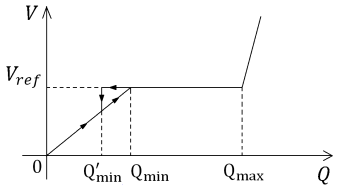

Fig. 2. $Q-V$ characteristics of a VIC.

II. Control of VIC

The control of VIC is implemented by PWM control with constant switching frequency 50kHz, and is divided into three parts according to the Q-V charateristics. Please refer to [3] for more details of the control scheme and duty cycle deduction. It is summarized in Fig. 3, and the $q^*, \tilde{q}^*$ are the duty cycle of two switches. Different from [3], in our experiment, the transitions between three processes are realized by the state machine. At the moment of transition, both switches in VIC are turned OFF for one period as the short-circuit protection. The expression of q^* and $\tilde{q}^*$ are shown as follows: power up process,

$$\begin{cases} q^* & = \frac{V_{s,min}}{V_{ref}}, \\ \tilde{q}^* & = 1 - q^*. \end{cases}$$

normal operation process,

$$\begin{cases} q^* & = \sqrt{\frac{2Li_p^*}{(V-V_s)T}} \\ \tilde{q}^* & = 0 \end{cases} \text{ if VIC in buck operation,}$$

$$\begin{cases} q^* & = 0 \\ \tilde{q}^* & = \sqrt{\frac{2L(V-V_s)|i_p^*|}{V_s^2 T}} \end{cases} \text{ if VIC in boost operation.}$$

protection,

$$\begin{cases} q^* & = 0, \\ \tilde{q}^* & = 0. \end{cases}$$

III. Simulation and Experiment Setup

Fig. 4 shows the circuit connection in the experiment. The VIC will remove the sinusoidal voltage provided by auto-transformer. Note that it can suppress random fluctuations, whereas, the periodical fluctuations is applied here for easy realization in hardware experiment. The diode D in Fig.4 prevents the current flowing back to DC voltage source for protection purpose. The resistor R_p serves as short circuit protection in case of wrong switch operation.

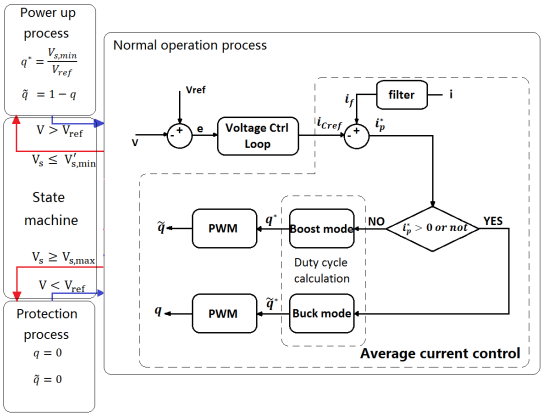

Fig. 3. Overview of the control logic with the state machine.

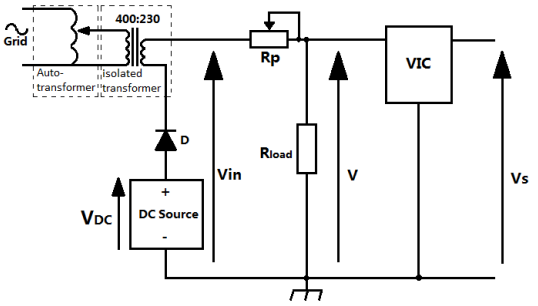

Fig. 4. Circuit of VIC experiment to suppress the periodical voltage.

By changing the DC voltage, the VIC may operate in different situations. When V_{DC} is small, the VIC will stay in power up process. Then, as the voltage V_{DC} increase to certain level, the VIC will operate in power up process and normal operation process, and switch to each other periodically. If we keep increasing the V_{DC}, the VIC will start to operate between normal operation process and protection process.

In simulations, when V_{DC} is approximately 214.7V, it will start from the power up process and stay in normal operation process for a few seconds, gradually rising to the protection process. Then it will operate in both normal operation stage and protection stage. This 'boundary' voltage is 214.3V in experiment.

TABLE I
Experiment Parameters and Electronic Device Set Up.

Para.	Setting	Device	Setting
V_{in}	$V_{DC} + 42.5\sin(\omega_g t)$	C	10 μF
ω_g	100π rad/s	C_s	40 μF
V_{ref}	200 V	R_{Load}	1000Ω
$V_{s,min}$	60 V	L	120 μH
$V'_{s,min}$	40V	R_p	100Ω
$V_{s,max}$	180 V	$C_{p1}C_{p2}$	158 pF
$V_{s_{ref}}$	93.4 V	R_{sn}	500Ω
		C_{sn}	1 nF

The experiment parameters and electronic components set up are shown in Table.I. The control algorithm is embedded into an off-the-shelf control card TMDSDOCKH52C1. A $12 \times 16cm$ four-layer PCB is

designed to implement VIC (see Fig. 5). Electrolytic capacitors are chosen for the capacitor C and C_s, with the voltage rating of $500V$. The experiment is set up according to the circuit in Fig. 4.

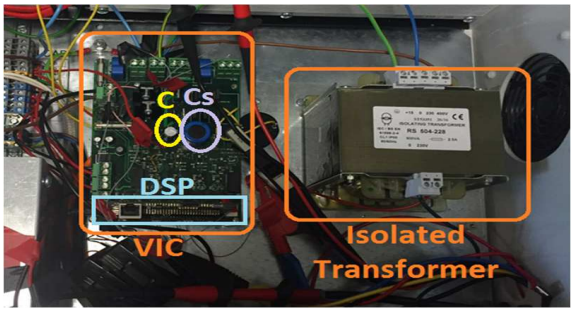

Fig. 5. Photo of VIC and its connections.

The voltage V, V_s and current i, i_s are sensed with low pass filter in the experiment. See Fig. 6 for the schematic diagram of the sensing circuits. The 'floating ground' is used for current sensor (denoted as F_GND in Fig. 6). The votlage drop between V_{sense}, V'_{sense} and F_GND are negligible, since the resistor R_1 is very small. Two 1st-order RC filters are applied to extract the clear average current signals. By chosing the suitable resistors and capacitors, the corner frequency of these two low pass filters are set to be around 5kHz and 1kHz respectively (see Table. II). One 1st-order RC filter is used to get rid of the high frequency noise in voltage signals. The corner frequency of this low pass filter is set to be around 5kHz (see Table III).

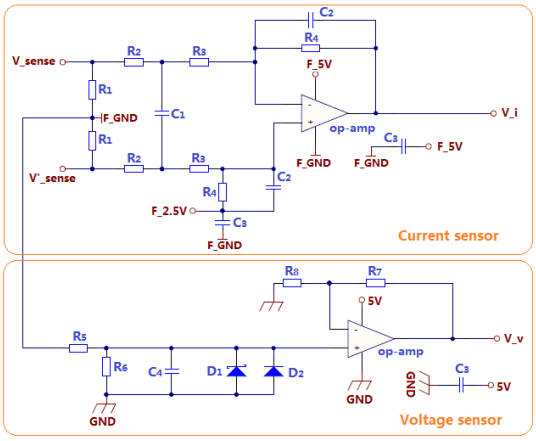

Fig. 6. Schematic diagram of the sensing circuit to obtain V, V_s, i, i_s signals for control card.

The current can flow in both directions in our experiment. We applied a floating 2.5V as the reference (denoted as $F\_2.5V$ in Fig.6). The current flowing in two directions will be shown as larger or smaller than 2.5V at sensor output. C_3 is a small capacitor to filter out the high frequency noise. The diode D_1 is the zener diode with nominal zener voltage of 5V to protect the op-amp. Equation (1) and (2) are the transfer functions of current sensor and voltage sensor.

$$V_i = i \cdot 2R_1 \cdot \frac{-R_4}{R_2+R_3} \frac{\frac{R_2+R_3}{2R_2R_3C_1}}{s+\frac{R_2+R_3}{2R_2R_3C_1}} \frac{\frac{1}{R_4C_2}}{s+\frac{1}{R_4C_2}} + 2.5V \quad (1)$$

TABLE II
RESISTOR AND CAPACITORS TO SENSE i AND i_s

Resistors in the sensing circuit of			Capacitors in the sensing circuit of		
	i	i_s		i	i_s
R_1	0.05Ω	0.05Ω	C_1	15nF	12nF
R_2	$2k\Omega$	$3k\Omega$	C_2	3.9nF	3.9nF
R_3	$2k\Omega$	$3k\Omega$	C_3	0.1μF	0.1μF
R_4	$40.2k\Omega$	$40.2k\Omega$			

TABLE III
RESISTORS AND CAPACITORS TO SENSE V AND V_s

Resistors in the V & V_s sensor circuits		Capacitors in the V & V_s sensor circuits	
R_5	$510k\Omega$	C_3	0.1μF
R_6	$3.3k\Omega$	C_4	10nF
R_7	$8.2k\Omega$		
R_8	$10k\Omega$		

$$V_v = V_{in} \cdot \frac{R_6}{R_5} \cdot \frac{R_7+R_8}{R_8} \cdot \frac{\frac{1}{R_6C_4}}{s+\frac{1}{R_6C_4}}. \quad (2)$$

IV. Simulation and Experiment Results

In this section, by changing V_{DC}, we show the performance of VIC operating in four different situations, see Fig. 7 and Fig. 8 for the simulation and experiment results respectively. The simulations are run under the same settings as that in experiments.

During the VIC's normal operation region (see Fig. 7(c) and Fig. 8(c)), the $85V$ voltage ripple is confined into a DC voltage by VIC with high frequency ripple of $1.5V$ in simulation, while it is around $7V$ in the experiment. The difference may due to some real scenarios which cannot be fully considered in simulation, such as the EMI, the device tolerance, etc. During the protection stage (see Fig. 7(d) and Fig. 8(d)), the voltage V_s becomes flat, which means that the capacitor C_s is no longer connecting to the circuit. It effectively protects the C_s from being overcharged.

It is clear that the VIC performance meets our expectations. No visible low frequency ripples appear in either simulation or experiment. The experiment results are highly consistent with simulations.

V. Conclusion

In this paper, we experimentally verified the ripple suppression performance of the modified VIC in [3] in a simple and straightforward way. The VIC is controlled to completely remove the $50Hz, 85V_{peak-peak}$ ripples voltage and successfully obtain the DC voltage at its output terminal. Our experiment results showed that the VIC performed very well, which were highly consistent with the simulation results. The experiment performance of VIC demonstrated the possibility to substitute the large filter capacitors with VIC in the industrial applications.

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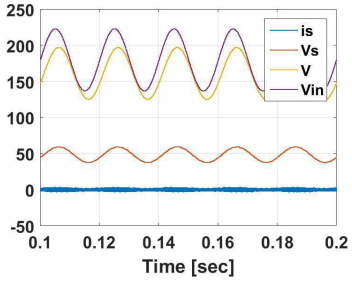
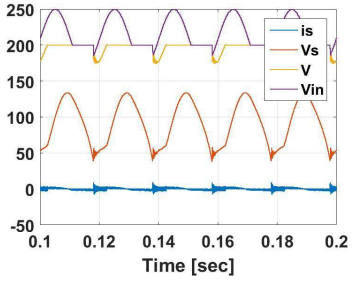
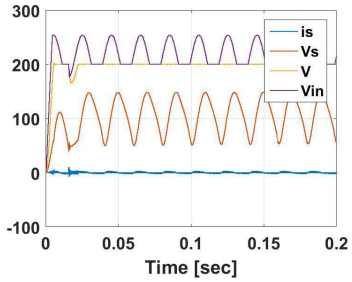


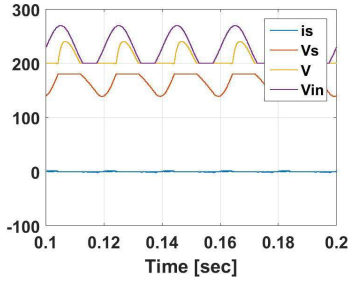
(a) Power up process, $V_{in} = 180 + 42.5sin(100\pi t)$.



(b) Power up & normal operation, $V_{in} = 210 + 42.5sin(100\pi t)$

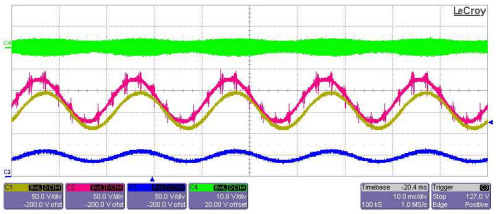


(c) Normal operation, $V_{in} = 214.7 + 42.5sin(100\pi t)$.

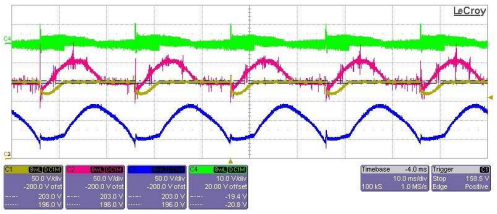


(d) normal operation & protection, $V_{in} = 230 + 42.5sin(100\pi t)$

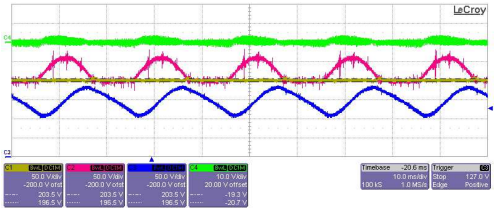
Fig. 7. Simulation results in four different situations.



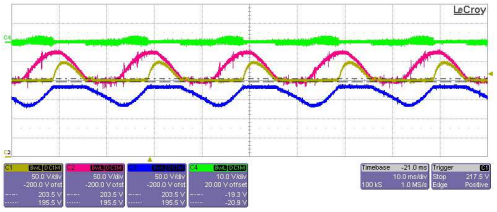
(a) Power up process, $V_{in} = 180 + 42.5sin(100\pi t)$.



(b) Power up & normal operation, $V_{in} = 210 + 42.5sin(100\pi t)$.



(c) Normal operation, $V_{in} = 214.3 + 42.5sin(100\pi t)$.



(d) normal operation & protection, $V_{in} = 230 + 42.5sin(100\pi t)$.

Fig. 8. Experiment results in four different situations. In the figure, the green, pink, brown, blue signals are i_s, V_{in}, V, V_s, respectively.

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