Performance Analysis of Monolithically Integrated Depletion-/Enhancement-Mode InAlN/GaN Heterostructure HEMT Transistors

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***Abstract*—The paper addresses a top-down design flow of depletion-load digital inverter formed by monolithically integrated depletion-mode and enhancement-mode high electron mobility transistors (HEMTs) on common InAlN/GaN heterostructure grown on sapphire substrate. We describe the inverter design at transistor level using HSPICE models developed earlier. The inverter layout representation, which also defines the lithographic masks required for the fabrication process, is presented as well. The proposed mask set was designed taking into account the *design-for-manufacturing* approach. Furthermore, we evaluated measured properties and performance of the fabricated transistors and circuits and recalibrate the transistor models according to the latest measurements.**

***Index Terms*—InAlN/GaN Heterostructure, Monolithic integration, HEMT transistor, Digital inverter**

I. INTRODUCTION

The interest in field-effect transistors fabricated on GaN heterostructure has risen tremendously in the last decade. Thanks to very promising properties of this III/V semiconductor compound and advances in technology, its application has shifted from optoelectronics only to power and RF domains as well. This material exhibits a wide energy bandgap, which predestines its application to high temperature, high voltage and harsh environment in general [1]. Furthermore, thanks to the two-dimensional electron gas (2DEG) channel, the HEMT transistors are also able to deliver high power at RF frequencies. The exceptional properties of active elements produced on GaN heterostructure, however, are compromised by the immaturity of the fabrication process, problems with monolithic integration of several devices onto a single die and the instability of the electrical parameters. In fact, the most suitable manufacturing steps are still under an intensive development.

In this paper, we discuss the monolithic integration of enhancement-mode and depletion-mode HEMT transistors on InAlN/GaN heterostructure, which according to the theory, promises the highest current densities and the best performance from all GaN heterostructures used in microelectronics so far [2]. The article is organized as follows. Section II describes a transistor level design of the simplest circuit employing both types of the HEMT devices, namely, a digital inverter. It also presents a design of the lithographic masks required for the manufacturing. Section III deals with the measured properties of the fabricated wafer and the re-calibrated HSPICE models. In section IV, the future research plans are presented, and some conclusions are drawn.

II. THE PROPOSED INVERTER TOPOLOGY

Fig. 1 depicts the proposed inverter circuit along with the dimensions of active devices. It represents a well-known *depletion-load* topology [3] that consists of the depletion-mode HEMT (D-HEMT) transistor M1 employed as a constant current source. We can also describe the role of M1 as a device that pulls the output node to the positive power supply rail. Its gate terminal is shorted out with the source terminal to ensure the driving voltage V_{GS} = 0 V. Hence, as soon as the drain-source voltage V_{DS} exceeds the saturation voltage, the transistor becomes a current source with only small voltage dependency. The current flow is either handled by the second transistor or by load connected to the inverter output. The dimensions of the described device have been chosen carefully, based on the detailed analysis and its results published in [4–6]. The enhancement-mode HEMT (E-HETM) transistor M2 acts as a low-side driver and it is responsible for pulling the output node to the ground. Several versions of the proposed logic inverter with various gate widths of the enhancement-mode transistor in order to investigate wider spectrum of circuit parameters and dependencies have been designed.

Fig. 2 shows the layout representation of the proposed monolithic integration of both HEMT transistor types. In this case, the enhancement-mode device gate was designed with the width of 25 μm. The design of lithographic masks was also taking into account possible fabrication deviations, following so-called design-for-manufacturing approach. Let us describe the major steps of the manufacturing process which has been developed at Slovak Academy of Sciences. The first

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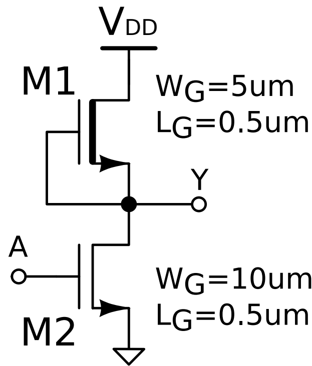

Fig. 1. Schematic diagram of the proposed digital inverter.

step is an ion milling in order to create the future active mesa region of both HEMT transistor types. The area of mesa region is deliberately enlarged in some places in order to minimize contact parasitic resistance. The second step is represented by forming

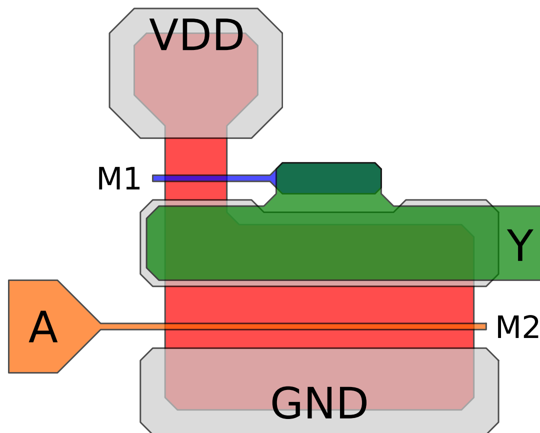

Fig. 2. Layout of the monolithic integration.

the ohmic contacts for drain and source terminals of the future transistors. Since the source terminal of the depletion-mode HEMT and the drain terminal of the enhancement-mode device are connected (at schematic level), a shared central contacts was designed. Again, contacts are overlapping the edge of mesa region in order to improve their dependability and reliability. The third and fourth process steps would create self-aligned transistor gates. The gate of the enhancement-mode device is incorporating a MOS structure, which requires an extra processing step. However, the same lithographic mask can be used that is rather beneficial. This is one of the main assets of the presented fabrication technology. The thickness of the MOS structure also determines the value of E-HEMT threshold voltage. The gate material is overlapping the mesa region in order to minimize the fringe parasitic effects. On the other hand, it should not overlap the region too much because of possible leakage current induction. The last step consists of creating the interconnecting metal layer between respective contacts or devices. One can observe the increased area of a short between the depletion-mode HEMT gate and the output terminal as well. The reason for this approach is again increased reliability of the contact. The whole layout design also took into account the possibility of further integration of multiple logic gates. Thus, the aspect ratio of the whole circuit, bonding metal layer and input/output terminals position were designed to resemble a classic digital standard cell. The specifics, technology details and more profound process description can be found in [7].

Fig. 3 depicts a micrograph of the manufactured monolithic integration of the depletion/enhancement-mode HEMT transistors based on the proposed lithographic masks (Fig. 2) and fabrication process described above. One can observe a shift of the mesa region in the manufactured inverter relative to the rest of the mask set. However, most of the proposed circuits presented on a wafer did withstand this unfortunate processing deviation thanks to a robust layout design. We can, therefore, state that the monolithic integration of both HEMT transistor types has been successful.

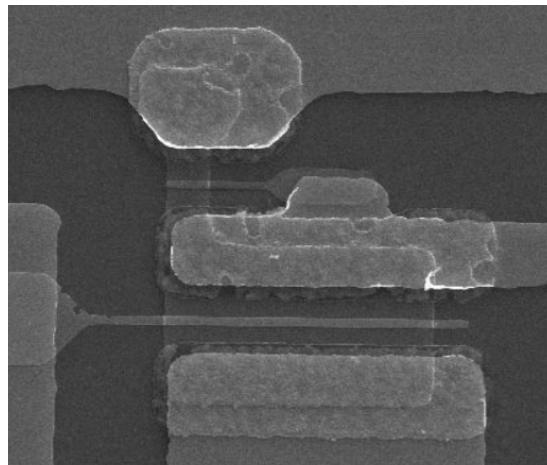

Fig. 3. Micrograph of the fabricated logic inverter.

III. MEASUREMENT RESULTS

The processed wafer has been extensively investigated by numerous testing procedures. From the designer's point of view, the most fundamental scrutiny that always needs to be performed is the DC measurement of the most vital parameters of the tested circuit. In our case, DC parameters such as transfer characteristics of standalone HEMT transistors, I-V characteristics of constant current sources, transfer characteristics of monolithic inverters, their current consumption and noise margin values were measured. All parameters presented in this section were measured by Agilent 4155C Semiconductor Parameter Analyzer. The first measurement on the wafer was performed on a stand-alone depletion-mode HEMT transistor. Fig. 4 shows the results of this evaluation. The transfer characteristics along with its derivative – the transconductance characteristics are depicted. The numerical analysis has determined the threshold voltage V_{TH} = -2.53 V. The bench data are interpolated by modified Angelov HSPICE model also developed

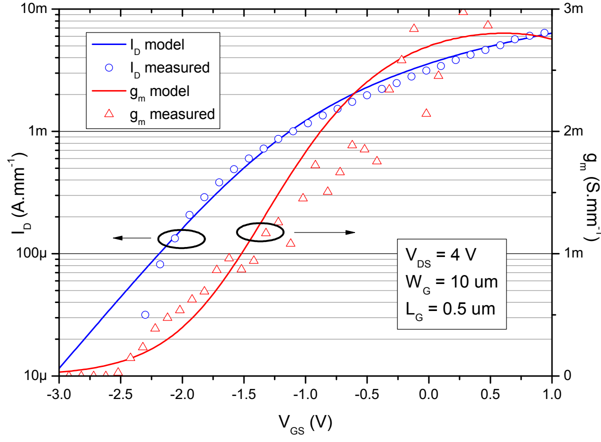

Fig. 4. Measured and modeled transfer and transconductance characteristics of D-HEMT transistor.

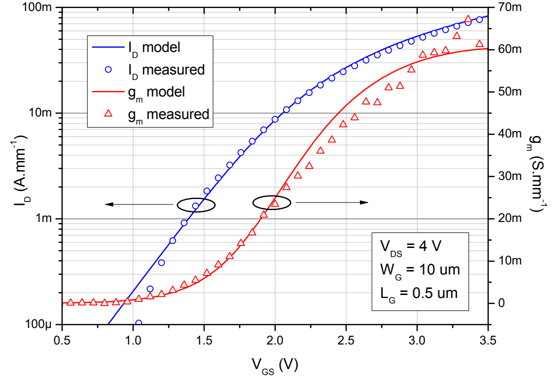

Fig. 6. Measured and modeled transfer and transconductance characteristics of E-HEMT transistor.

within our research [8]. The model accuracy is acceptable in the whole range of voltages above the threshold level. However, HSPICE models for the current source and E-HEMT device exhibit exceptional accuracy.

Fig. 5 depicts measured I-V output characteristics of the depletion-mode HEMT transistor employed as a constant current source. The waveform is essentially the output I-V characteristics of the respective device at room temperature for V_{GS} = 0 V. The saturation voltage for given configuration is roughly about V_{Dsat} = 2.75 V. One can observe almost ideal accuracy of the transistor model, with the worst-case discrepancy of only 0.59 % in the saturation region.

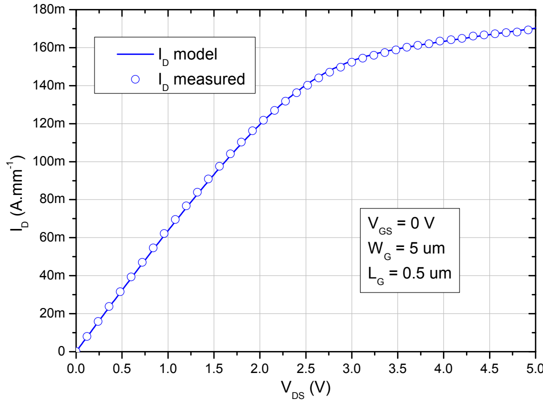

Fig. 5. Measured and modeled output characteristics of D-HEMT device employed as a constant current source.

The measured transfer characteristics along with the transconductance of the enhancement-mode transistor are shown in Fig. 6. The measured data were obtained at room temperature. The developed model interpolates the experimental data with outstanding accuracy, where the worst deviation of 7.54 % for voltages above the threshold voltage V_{TH} = 1.21 V is reported. The transconductance curve was realized by deriving the transfer characteristics.

After measurement of the separate devices, we continued to investigate the behavior of the digital inverter itself. Fig. 7 depicts the measured transfer characteristics along with the current consumption of a single inverter of the proposed topology. The experiment was performed at room temperature and with the power supply voltage 4 V. This value has been chosen to ensure that the depletion-mode transistor would be working in saturation region (Fig. 5). Due to smaller transconductance values of the low-side driver transistor, the voltage for logic zero is higher than expected. In other words, the enhancement-mode device is not able to pull the output node closer to the ground potential and therefore, the output swing of the inverter is slightly reduced. The developed models

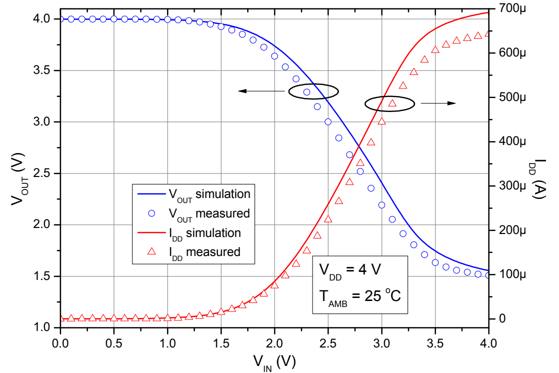

Fig. 7. Measured and modeled transfer characteristics along with the current consumption of the proposed digital inverter.

for respective devices were also used for simulating the various characteristics of the inverter. One can observe a tight correlation between measurement and simulation results for the transfer characteristics as well as the current consumption. Despite the undesired raised voltage representing the low logic state, the noise margins extracted from the measured data remain positive. Namely, the noise margin value for the high logic state NM_H = 387 mV, its counterpart NM_L = 138 mV and the maximum of voltage gain A_V = 1.75. Therefore, multiple inverters could be connected in series and the logic function would remain in tact. Furthermore, this also enables a creation of ring oscillator

formed by an odd number of inverters with the output voltage amplitude of 2.5 V (for the presented value of the supply voltage). It also enables implementation of the inverter as an analog amplifier in mixed-signal circuits as well.

IV. Conclusion

We have demonstrated a successful top-down design flow of the digital inverter on InAlN/GaN heterostructure which is consist of two monolithically integrated HEMT transistors with different threshold voltages. Presented fabrication process introduces a great advantage in terms of manufacturing steps reduction and thus, overall simplification while maintaining successful feasibility. The aspect ratio of both transistors was determined by the research and development carried out previously. The layout and lithographic masks design represented a critical step in terms of robustness and tolerances. We can state that is was done correctly and successfully. An unfortunate fabrication deviation of mask shift has occurred, however, measured circuits still exhibit satisfactory parameters despite its negative impact. The processed wafer has been verified by numerous analytical methods, but from designer's point of view, the basic DC parameters represent a sufficient verification of the proper function. In our case, the transfer characteristics of both types of standalone HEMT transistors were measured, as well as the depletion-mode constant current source. Afterwards, the transconductance characteristics were derived. With the bench data, previously developed HEMT transistor HSPICE models were re-calibrated for purposes of the future research and transistor level design. The measurement of digital inverter circuit which demonstrates a functional monolithic integration of both transistor types includes its transfer characteristics and its overall current consumption. The derived parameters such as noise margin, voltage gain and logic input/output voltage levels have indeed confirmed successfully fabricated design. The re-calibrated HSPICE models have also shown a tight correlation between measured and simulated characteristics. These results support the previous statement even further, since it implies the possibility of connecting several inverters in series with maintained logic function. Another important contribution we obtained is the optimization of the manufacturing process for the future run. We projected a refined values of threshold voltages for both HEMTs in order to improve the logic gates properties.
Our future research will include the investigation of a 3-stage inverter and various different combinatorial logic gates using the same circuit topology. We would also like to characterize the 5-stage ring oscillator and sequential RS flip-flop circuit which executes the memory function.

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