GaN Based Inverter Current-Collapse Loss Decrease Using 5-segment Modulation

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***Abstract*—The current collapse phenomenon increases conduction losses in high electron mobility transistors. This paper presents a simple option to decrease these losses in 3 phase hard-switching inverter driving permanent magnet synchronous motor utilizing 5-segment SVPWM modulation. Converter DC-link input power decrease by 2 % was observed compared to classic 7-segment modulation. This decrease results in significant decrease of transistor operating temperature.**

Keywords—GaN, current-collapse, 3-phase inverter, PMSM

I. Introduction

High electron mobility transistors achieving high efficiency and high power density in power converters these days [1]. There are several problems limiting their usage in drives. From hardware point of view there is complicated circuit board layout due high dv/dt of high speed switching that is also limiting parts selection for DC-link capacitors, drivers, measurement devices or insulation barrier [2]. Also when controlling switching of GaN transistors we have to optimize the control such as minimum deadtime for using the channel conducting reverse current to minimize reverse conduction loss [3]. Another problem which is studied in this paper is further, to study the current-collapse phenomenon which increases the conduction loss of hard-switched converters operating at high switching frequencies [4].

There are transistors in development that minimizes the current-collapse loss [5] however the transistors available today on the market have this problem and we have to take it in account when designing the converter. Due current-collapse GaN transistors produce more heat than calculated from datasheet steady state parameters [6].

The typical hard-switched GaN based topology of 3-phase motor voltage source inverter (VSI) is as shown in Fig. 1. Hard switching means that each transistor has blocking voltage equal to the supply DC-link voltage across drain-source the whole time the transistor is turned off. The voltage on the output is commutated by the transistor turning-on which also switch the current path.

This topology is widely used due the simplicity. Fast transistors such as GaN brings the advantage of low switching losses even at higher switching frequencies in hard-switched converters.

In recent papers the current-collapse losses are being studied from the transistor's point of view while this paper tries to minimize this loss in a converter made of transistors available on the market.

The method used is change in the controller's software adjusting the modulation to lower the amount of time the current-collapse losses appears.

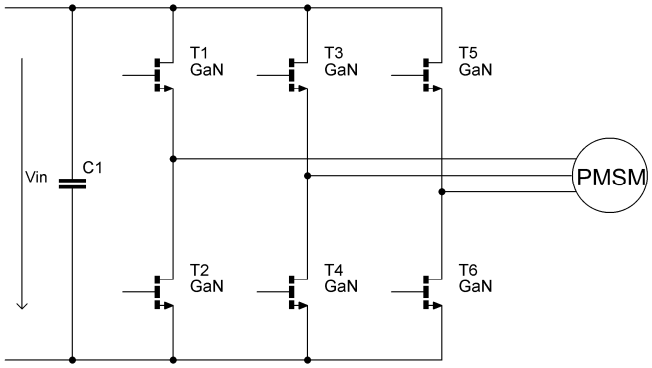

Fig. 1. Inverter topology

II. Theory

A. Current Collapse Phenomenon in GaN Structure

In the structure [7] of GaN transistor in Fig. 2 the channel current depends on the transistor transconductance, applied gate voltage from driver and the threshold voltage [8] according to (1).

$$i_{\mathrm{ch}} = g_{\mathrm{m}}(V_{\mathrm{GS}} - V_{\mathrm{th}}), \tag{1}$$

where i_{ch} is channel current, g_m transistor transconductance, V_{GS} applied gate-source voltage and V_{TH} threshold voltage of the transistor.

Current collapse phenomenon we called the state when trapped charges creates a charged layer around the gate that decreases the transconductance and increases gate threshold right after the transistor is turned on again [9]. It takes some time for the trapped charges to be removed and during this time the on state resistance R_{DSon} is higher than the datasheet value. The trapped charges are present there when the structure is stressed with blocking voltage when the transistor is turned-off.

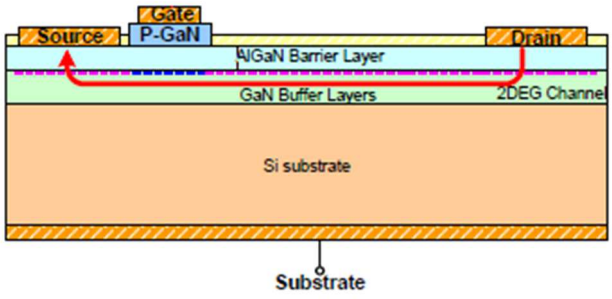

Fig. 2. Structure of GaN transistor [7]

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In hard-switching topology from Fig.1 there is blocking voltage present on the transistor right before turning on. This makes the current-collapse phenomenon occurring in such topologies mainly. Operating in high dynamic on state resistance decreases the efficiency of the converter.

The behavior of dynamic on-state resistance is depicted on the Fig. 3. It illustrates both the dependence on time and blocking voltage level. This behavior was observed in static measurement presented in [10].

There are several possible solutions how to minimize this problem that are summarized in Table 1.

The blocking voltage before turn-on can be decreased using zero voltage switching in resonant converters for example [11]. Decreasing switching frequency helps to leave more time for the on state resistance to decrease too.

For this paper we selected to adjust the modulation to decrease the loss created by current collapse phenomenon.

B. 5-Segment SVPWM

Space vector pulse width modulation (SVPWM) is widely used in motor control for its ability to maximize the utilization of DC-link voltage. There are multiple patterns how to form the output converter's voltage [12]. However, nowadays the most often used is the 7-segment modulation. This is due to minimizing current ripple for given switching frequency.

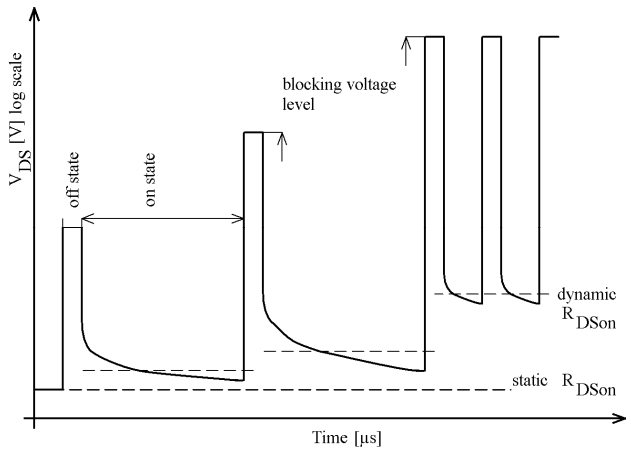

Fig. 3. Static and dynamic on-state resistance behavior with current-collapse phenomenon

Table 1. Current-collapse problem and possible solutions

Problem	Cause	Possible solution
Blocking voltage	More trapped charges increases R_{DSon}	Soft-switching
		DC-link voltage regulation
Time since turn-on	Less time to remove the charges to decrease R_{DSon}	**5-segment modulation**
		Decrease switching frequency

With high speed switching wide band-gap transistors, we can increase the switching frequency and utilize the other types of modulation without increasing the current ripple through the motor windings. The main benefit of 5-segment modulation is lower number of turn-on transitions per period.

The control circuit in Fig. 4 shows a classic PMSM control loop in dq-frame. The speed control loop was added just for measuring purposes.

The control SW is written such that the modulator can be reconfigured from 7-segment to 5-segment at any time while the motor is running. With this a proper data measurement can be achieved minimizing offsets when starting the drive multiple times.

The modulator recalculates the demanded abc voltages from the 2-3 transformation into the actual duty cycle values sent to the VSI. In case of 7-segment modulator the rotation frame is divided into 6 sectors depending on the demanded voltage values v_{abc}. The VSI duty cycles d_{abc} are calculated according to (2-4).

$$v_A > v_B > v_C \quad \text{or} \quad v_C > v_B > v_A \begin{cases} d_A = \frac{(v_A - v_C)}{2v_{DC}} \\ d_B = \frac{(2v_B - v_A - v_C)}{2v_{DC}} \\ d_C = \frac{(v_C - v_A)}{2v_{DC}} \end{cases}, \quad (2)$$

$$v_B > v_A > v_C \quad \text{or} \quad v_C > v_A > v_B \begin{cases} d_A = \frac{(2v_A - v_B - v_C)}{2v_{DC}} \\ d_B = \frac{(v_B - v_C)}{2v_{DC}} \\ d_C = \frac{(v_C - v_B)}{2v_{DC}} \end{cases}, \quad (3)$$

$$v_A > v_C > v_B \quad \text{or} \quad v_B > v_C > v_A \begin{cases} d_A = \frac{(v_A - v_B)}{2v_{DC}} \\ d_B = \frac{(v_B - v_A)}{2v_{DC}} \\ d_C = \frac{(2v_C - v_A - v_B)}{2v_{DC}} \end{cases}, \quad (4)$$

In case of 5-segment modulation we search which demanded voltage is the lowest at time and we set the respected duty cycle to zero. The rest duty cycles are calculated according to (5-7) such that the VSI output voltage respects the originally demanded value, same as for the 7-segment modulation.

Resulting switching pattern depending on type of modulation is in Fig. 5 and the reference duty cycles in Fig. 6 and Fig. 7 together with the output voltage between phases which is the same for both type of modulations.

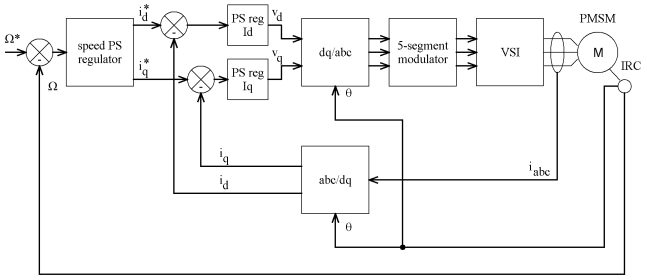

Fig. 4. Control schematic diagram

$$v_A > v_B > v_C \text{ or } v_B > v_A > v_C \begin{cases} d_A = \frac{(v_A - v_C)}{2v_{DC}} \\ d_B = \frac{(v_B - v_A)}{2v_{DC}}, \\ d_C = 0 \end{cases} \quad (5)$$

$$v_C > v_A > v_B \text{ or } v_A > v_C > v_B \begin{cases} d_A = \frac{(v_A - v_B)}{2v_{DC}} \\ d_B = 0 \\ d_C = \frac{(v_C - v_B)}{2v_{DC}} \end{cases}, \quad (6)$$

$$v_B > v_C > v_A \text{ or } v_C > v_B > v_A \begin{cases} d_A = 0 \\ d_B = \frac{(v_B - v_A)}{2v_{DC}} \\ d_C = \frac{(v_C - v_A)}{2v_{DC}} \end{cases}, \quad (7)$$

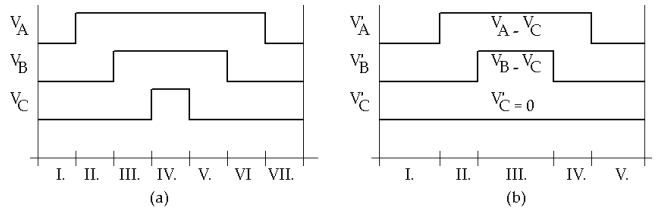

Fig. 5. Modulation techniques (a) 7-segment and (b) 5-segment

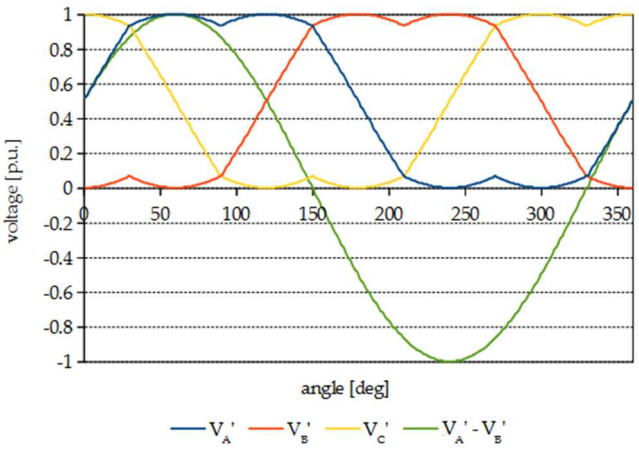

Fig. 6. Modulator reference phase voltages in 7-segment modulation

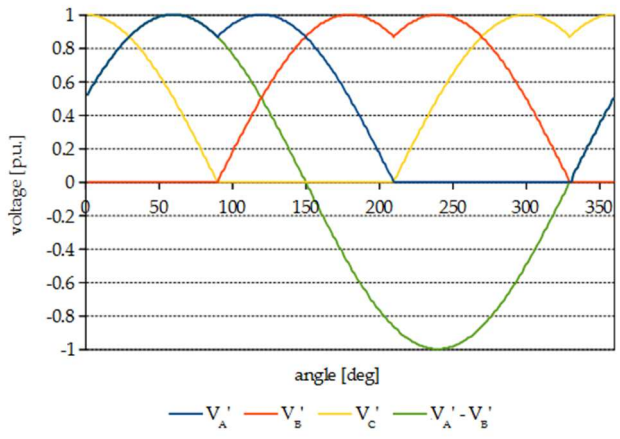

Fig. 7. Modulator reference phase voltages in 5-segment modulation

III. Experimental Setup

The experimental workplace as shown in Fig. 7 is consisted of DC voltage source, GaN based inverter, motor and generator with resistive load.

The inverter is using six GS66516B bottom cooled GaN transistors (650 V, 60 A, 25 mΩ). They are controlled by fast isolated halfbridge drivers Si8275. The C0G ceramic capacitor visible at each halfbridge closes the local current loop helping to achieve a clean switching. Phase currents are measured using TMCS1100 current sensors providing low offset values due their integrated temperature compensation.

On the upper side of the board there is a microcontroller ARM Cortex M4 STM32F334 containing the motor control loop from Fig. 4. This microcontroller is optimized for high frequency switching converters due to the sub-nanosecond timer resolution.

The converter is running at 100 kHz switching frequency while the calculation of the control scheme runs at 50 kHz.

The inverter is driving 500 W 4-pole permanent synchronous motor (PMSM) which is coupled to the same machine used as a generator into a resistive load.

IV. Measured Data

The measured data from the microcontroller are shown in Fig. 9 and Fig. 10 for both modulation techniques. Collected data for each calculation period were stored in the memory and transferred out through serial bus.

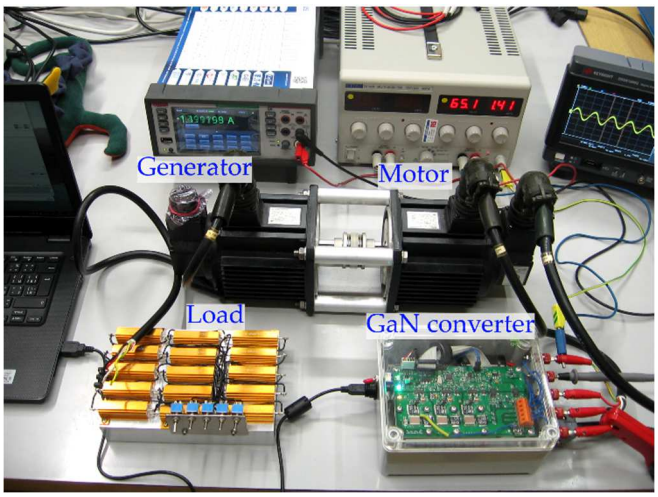

Fig. 8. Experimental workplace

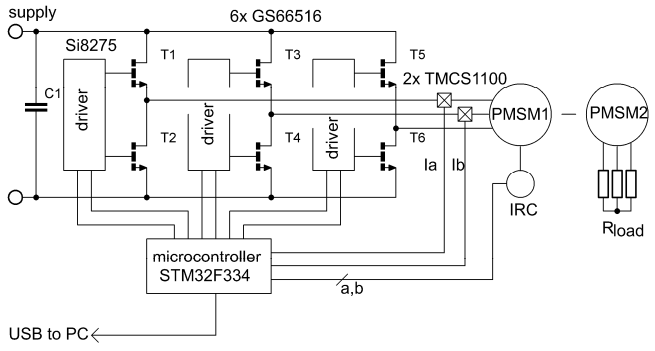

Fig. 9. Experimental workplace schematic diagram

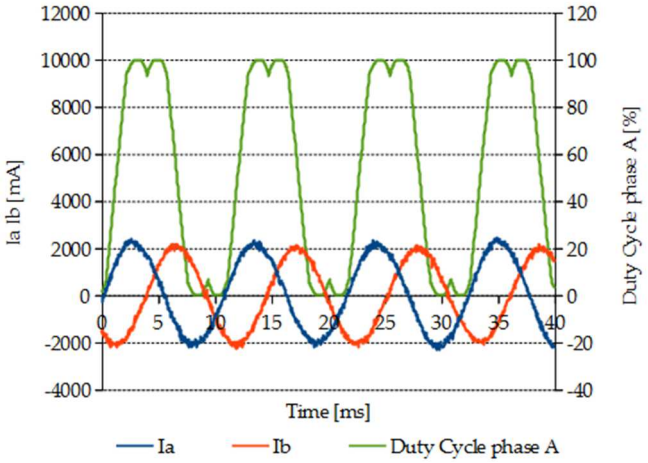

Fig. 10. MCU data 7-segment modulation

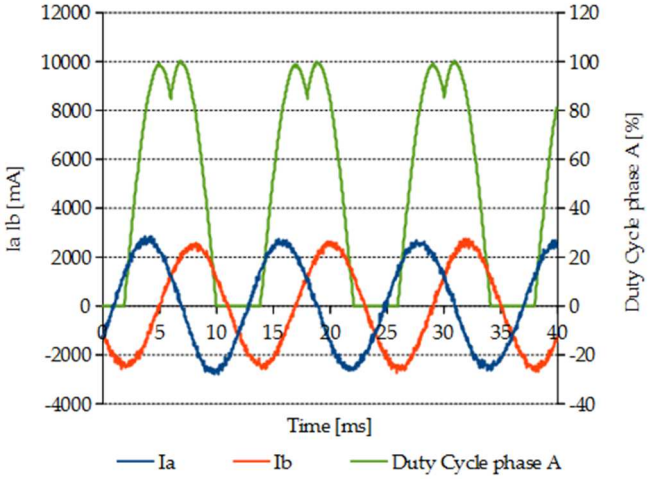

Fig. 11. MCU data 5-segment modulation

Fig. 10 and Fig. 11 clearly shows the difference between 7-segment and 5-segment modulation on the phase voltage reference curve. Phase current remains sinusoidal in both cases as there is no difference in shape of the voltage between phases when the modulation is changed.

Measurement with thermal camera was performed to see the difference in steady state temperature of GaN power transistors on the converter board. Operation point was set to 1400 RPM and 50 Ω load resistor

Measurement was done such way that the converter was running with 7-segment modulation until the temperature stabilized. Then it was reconfigured to 5-segment and after the temperature stopped dropping the Fig. 13 was taken. Then it was reconfigured back to 7-segment and when the temperature stabilized again the Fig. 12 was taken. This procedure minimizes the possible error of determining the steady state at the first time.

The Fig. 14 shows the converter board in detail for reference.

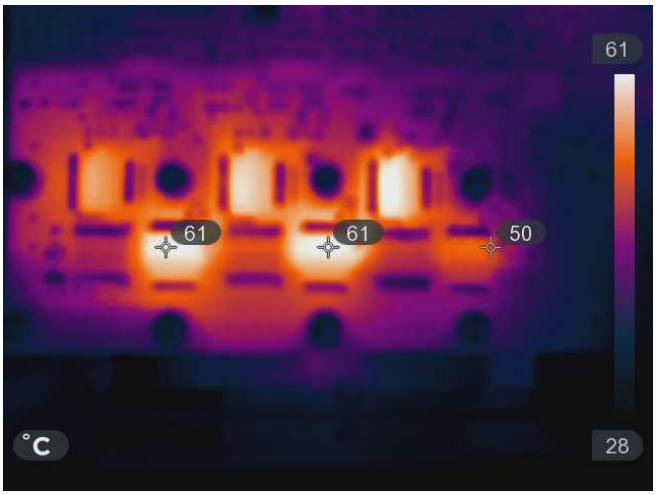

Fig. 12. Thermal image with 7-segment modulation

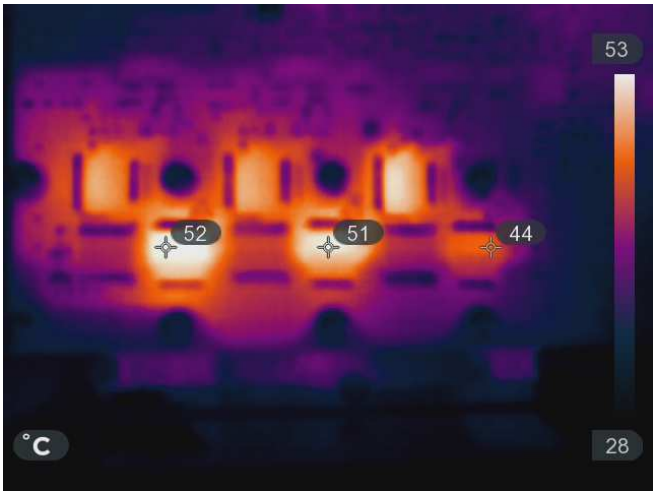

Fig. 13. Thermal image with 5-segment modulation

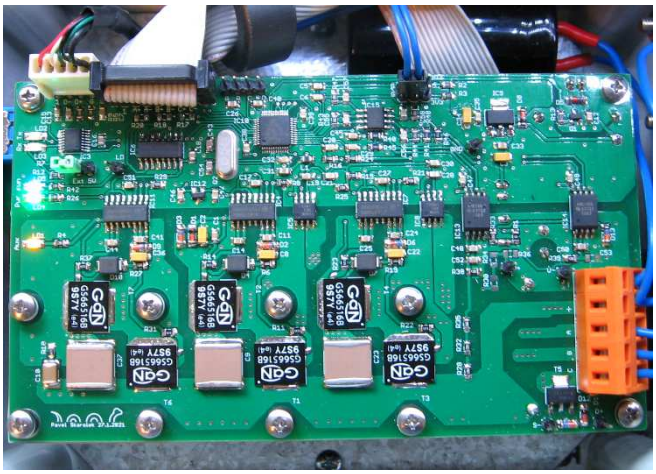

Fig. 14. GaN based converter board detail

To determine the loss decrease the input DC-link current at constant input voltage of 100 V and speed was measured in multiple steady state operation points of the drive. The results with calculated input power decrease are in Table 2.

Table 2. Measured DC-link input current

RPM	R load [Ω]	7-segment [A]	5-segment [A]	Decrease [%]
1200	200	0.313	0.295	6.1
1200	50	1.050	1.026	2.3
1400	200	0.380	0.362	1.8
1400	50	1.355	1.335	1.5

V. CONCLUSION

The current-collapse increases conduction losses in the GaN based converter. This loss increase is significant and we have to take it in account when designing the converter. Current-collapse free transistors are under development, but these available on the market today still have this problem. It means we still have to deal with this problem and oversize GaN converter's cooling system.

There are however a few options how to minimize this additional loss in an existing converter. The one presented in this paper is control software adjustment of the modulation. Based on the measurement changing the modulation from 7-segment to 5-segment decreases the losses in GaN based motor converter. Thermal images of the converter show significant decrease of the transistor's operating temperature.

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